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High linearity analog and mixed-signal integrated circuit design

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by

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ABSTRACT

Linearity is one of the most important specifications in electrical circuits. Designing a high linear analog circuit is always a challenging task and it is becoming even more difficult with the shrinking feature size and reducing supply voltage of modern standard CMOS process. Furthermore, the behavior characteristics of the transistor below sub-micro are not accurately described by the traditional BISM models. All those tendencies increase the difficulty to build the high performance analog circuits with satisfied distortion level, especially when the linearity relies mostly on active elements. In this dissertation, our research for achieving high linear analog circuits will be presented including a high linear analog active filter, a linear current mode digital to analog converter and a comprehensive study of calibration algorithms for improving the linearity of pipeline analog to digital converters.

There are total 6 Chapters in this thesis to conduct the research of high linearity analog integrated circuit design.

In Chapter 1, a ladder-based transconductance networks has been adopted first time to build a low distortion analog filters for low frequency applications. Polysilicon resistors have been known for its attractive linearity and have been used to build high linear analog active filters for medium frequency applications. However, due to the prohibit area for implementing the polysilicon resistors, there are very seldom applications of poly resistors in low frequency range. This new technique eliminated the limitation of the application with the traditional passive resistors for low frequency applications. We investigated the relationships between the transconductance networks and the opamp design so that with other circuit

components. Based on the understanding of this relationship, a strategy for designing high linear analog continuous-time filters has been developed. According to our strategy, a prototype analog integrated filter has been designed and fabricated with AMI05 0.5 um standard CMOS process. Experimental results proved this technique has the ability to provide excellent linearity with very limited active area and thus show the high agreements with our research works.

In Chapter 2, the relationships between the transconductance networks and major circuit specifications have been explored. The analysis reveals the trade off between the silicon area saved by the transconductance networks and the some other important specifications such as linearity, noise level and the process variations of the overall circuit. Further study of the trade off behavior, the mapping between the performance space and parameter space has been addressed. The close form expressions provide the systematic guide for using those transconductance networks with other specifications considerations. Experimental results of discrete component circuit matched very well with our analytical outcomes to predict the change of linearity and noise performance associated with different transconductance networks.

The Chapter 3 contains the analysis and mathematical proves of the optimum passive area allocations for several most popular analog active filters. Because the total area is now manageable by the technique introduced in the Chapter 1, the further reduce of the total area will be very important and useful for efficient utilizing the silicon area, especially with the today's fast growing area efficiency of the highly density digital circuits. This study presents the mathematical conclusion that the minimum passive area will be achieved with the equalized resistor and capacitor.

In the Chapter 4, a well recognized and highly honored current division circuit has been studied. Although it was claimed to be “inherently linear” and there are over 60 published works reported with high linearity based on this technique, our study discovered that this current division circuit can achieve, if proper circuit condition being managed, very limited linearity and all the experimental verified performance actually based on more general circuit principle. By pointing out what really support the high linearity, the circuit and system design community will eventually benefit from this research. Besides its limitation, our extended work, however, invented a novel current division digital to analog converter (DAC) based on this technique. Benefiting from the simple circuit structure and moderate good linearity, a prototype 8-bit DAC was designed in TSMC018 0.2 um CMOS process and the post layout simulations exhibited the good linearity with very low power consumption and extreme small active area.

As the part of study of the output stage for the current division DAC discussed in the Chapter 4, a current mirror is expected to amplify the output current to drive the low resistive load. The strategy of achieving the optimum bandwidth of the cascode current mirror with fixed total current gain is discussed in the Chapter 5. Our analysis provides an efficient way to improve the total bandwidth without adding any extra hardware. Simulations proved our strategy can efficiently increase the current mirror bandwidth by 10 to 25 percent compared to the previous works.

Analog to digital converter (ADC) is known as the largest volume mix-signal circuit in the world. Pipeline structure is one of the most popular structures in the ADC market for its high resolution and fast operation speed. It has been widely used in data acquisition system, communication system, etc. Improving the linearity of pipeline ADC has been the

hottest and hardest topic in solid-state circuit community for decade. Due to the physical limitation inherent in the semiconductor process, the linearity of the pipeline ADC is always limited within 14 bit level without calibrations. Thus lots of research activities have involved in the pipeline ADC design focusing on the calibration job to break this limitation. There are many published works to discuss different calibration schemes in the last 15 years and no real effective one really appeared. In the Chapter 6, a comprehensive study focus on the existing calibration algorithms for pipeline ADCs is presented. The benefits and limitations of different calibration algorithms have been discussed. Based on the understanding of those reported works, a new model-based calibration is delivered. The simulation results demonstrate that the model-based algorithms are vulnerable to the model accuracy and this weakness is very hard to be removed. From there, we predict the future developments of calibration algorithms that can break the linearity limitations for pipelined ADC.

CHAPTER 1 LOW-DISTORTION CONTINUOUS-TIME FILTERS FOR LOW FREQUENCY APPLICATIONS

1.1 Introduction

Filters are refer to those circuits that stimulate gain-frequency or phase-frequency relationship, some applications stimulate both. Active filters are the most popular technique to handle the analog signal instead of the passive filter due to the follow reasons: a) Passive filters are very sensitive to the component values; b) Passive filters cannot provide the gain itself; c) A first or second order filter cannot provide adequate roll-off.

Analog active filters are used from the very beginning stage of the electrical engineering field and also widely used in almost all kinds of applications today; anti-aliasing and reconstruction in data acquisition systems, channel selection in communication systems and so on. Today's analog filters are mainly implemented by the following techniques: g_m-C filters, Switched-Capacitor filters, Active-RC filters, MOSFET-C filters. The following table summary the applications and limitations of those techniques mentioned above.

Table1- 1 Popular filter techniques summary

Frequency Range	Spec.	gm-C	Switched-C	Active-RC	MOSFET-C
Low frequency	power	low	Low	low	low
	Linearity	poor	good	Very good	poor
	Area	Very large	Very large	Very large	small
Medium frequency	power	Low	Medium	Medium	Medium
	Linearity	Poor	good	Very good	poor
	Area	Large	large	Medium	small
High frequency	power	low	Difficult	High	low
	Linearity	poor		Very good	poor
	Area	small		small	small

Analog continuous time filters are used in many mixed-signal integrated circuits today. Of particular interest are integrated continuous-time filters that can be used for anti-aliasing and reconstruction in many large scaled DSP chips, which require high linearity to match the dynamic range of the DSP. Also continuous time filters are widely used in video processing systems, communications circuits, and audio applications. Linearity requirements for those applications are 40~50 dB, 60~70 dB and above 90 dB, respectively. One of the most popular traditional solutions for continuous-time filters are the MOSFET-C filters [1]-[5], in which a MOS transistor operating in the triode region replaces the passive resistor and this structure is easy to implement with operational amplifier while maintaining what of traditional active RC filters. Another well established technique is g_m-C filters [6]-[10]. However, there are two major limitations inherent in above proposed architecture which are hard to be overcome. The first limitation is the resistance or g_m value of MOS transistors' dependency on the process and temperature and this random variation causes the designed corner frequency to deviate without good prediction. Another limitation is the poor linearity and this limitation is mainly due to the voltage dependence inherent in the behavior of the MOS transistors. So this limitation is hard to be eliminated and there is no known good solution for high linear applications. From the previous works, most g_m-C filters and MOSFET-C filters can only achieve THD of about 40~60 dB [1]-[10]. The frequency deviation has been well compensated by several reported tuning algorithms [2]-[3], [5]-[7], [11]-[18], and it will not be discussed further in this chapter. The work presented in this work is focused on overcoming the second limitation.

It is well known that the passive components exhibit very low voltage dependence. Of the layers commonly available in CMOS process, polysilicon offers by far the most linear

resistors, (about 100 ppm/V) [19]. This is the reason for the fact that, compared to the g_m-C and MOSFET-C filters, RC filters exhibit much better linearity [14]-[16]. However, when RC filters require specific low-frequency poles, for example in kilo Hz range, the die area for integrating the corresponding large RC time constants will be a formidable undertaking. That is the reason that RC filter is seldom used in audio frequencies and always used in higher frequency range to achieve high linearity [15], [16]. Star-Biquad, for example, will occupy over 3 mm^2 for its RC time constants with the corner frequency set at 1 KHz. This area is almost unacceptable with the nowadays tendency that more area is allocated to advanced developed digital circuit for higher area efficiency in the mixed-signal systems or SOC. On the other hand, it is the low-frequency applications (i.e. audio and telecommunications) that require the highest linearity. Another factor limits the practical implementation of polysilicon resistors is the power requirement for driving small resistance load for reasonable signal level is quite high. Therefore, the solution for realizing large linear resistance with dramatically shrunk area is of particular interest.

In this Chapter, a method of implementing large value resistance with high linearity and significantly reduced area is introduced. The relationship between this proposed technique and non-ideal opamp is the highlight and a prototype filter is presented in the following section as an example for the practical RC active filter design. Experimental results agree favorably with the theoretical development of this proposed technique.

1.2 Proposed Transconductor Technique

Although the availability of a standard two-terminal resistor would be of particular interest, resistors are often used to realize a linear transresistance function. A first order low-pass filter is presented here as an example.

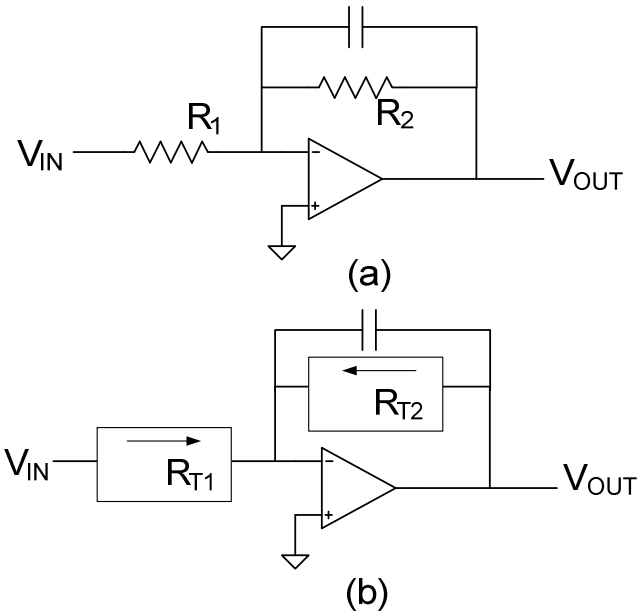

Figure 1- 1 -- First Order Low Pass RC Active Filter

In Figure 1-1(a), the ideal transfer function of output/input voltage is given by (1-1):

$$A_V = -\frac{R_2}{R_1}. \qquad (1\text{-}1)$$

Both R_1 and R_2 have one end connecting to the virtual ground of the operational amplifier and therefore, the real factors of those resistors important to this circuit is the transfer function between the input voltage and output current at the summing node. As shown in Figure 1-1(b), the voltage gain from output node to input node is:

$$A_V = -\frac{R_{T2}}{R_{T1}}. \qquad (1\text{-}2)$$

R_{T1} and R_{T2} are the transconductance gains of the input and feedback blocks respectively. This implicates that with the same linear transfer function of V_{in} and I_{out} for both input and feedback blocks, the whole circuit will achieve the same overall voltage gain no matter how to implement it.

Several possible implementations for resistors are shown in the Figure 1-2.

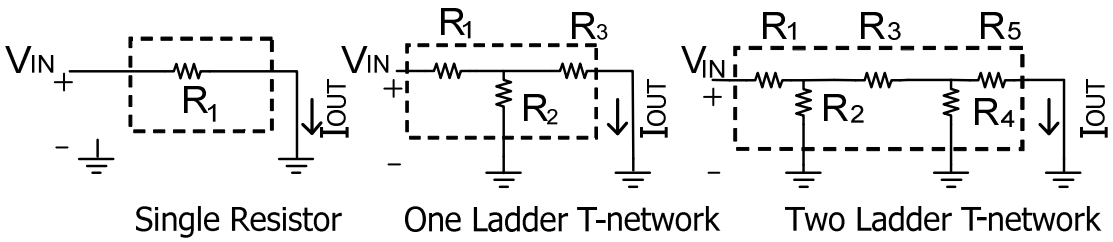

Figure 1- 2 – Three Implementations of Transconductance Gain.

The second architecture was termed as T-network [20] in literature. If proper values of R_1-R_5 are chosen, the three networks above will achieve the same transconductance value, which means that they will have the same transfer function of the input voltage and output current, the same linearity but progressively scaled area. The total resistance of $R_{1\sim3}$ and $R_{1\sim5}$, in T-network and Ladder network, respectively, are much smaller than the single resistor. The numerical example of those resistors' values is tabulated in Table 1-2.

Table1- 2 Numerical Examples of Implementation of Transconductance Networks

Trans	networks	R1	R2	R3	R4	R5	Total- R
1 M	single R	1 M					1 M
1 M	T-network	10 K	100	10 K			20.1 K
1 M	2 Ladder	500	12	500	12	500	1.524 K

1.3 High Linear Integrator with Transconductor Networks

1.3.1 Transconductance Networks and Open-loop Gain of Opamp

From the previous section, it is clearly shown that with ladder-based transconductance networks, small resistors can replace a large value resistor for achieving the same transfer function and thus the purpose of reducing area is obtained. However, the performance of the whole circuit may be changed since those transconductance networks eventually changed the architecture of the circuit. Understanding the relationship between the performance of the circuits and the structure of the transconductance networks becomes necessary and this study leads to the practical design which will compensate those negative impacts raised by introducing the area scaling method mentioned above.

It is well known that the non-ideal opamp is usually the key building block in the electrical circuit and degradation of the performances is related to those non-idealities of the opamp. Therefore, the first analysis will focus on the correlation between the transconductance network and open-loop gain of the opamp for the DC performance of highly linear integrators.

A simple resistor feedback circuit is used here as an example as shown in Figure 1-3.

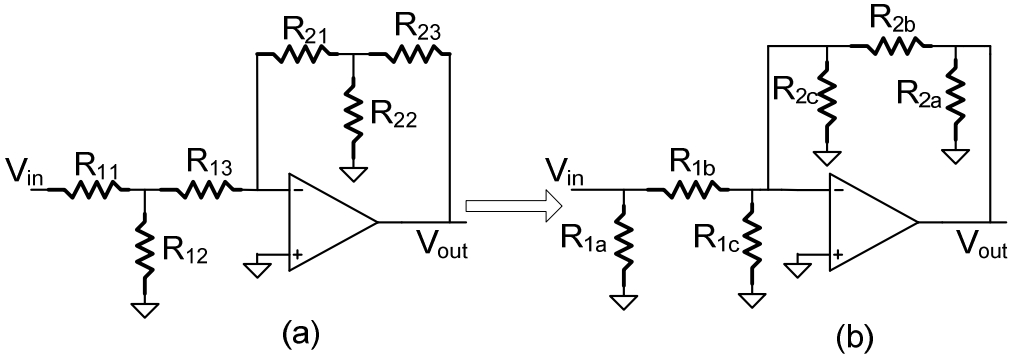

Figure 1- 3 -- Y-Δ Transformation of a Resistor Feedback Amplifier.

As shown in Figure 1-3, the Y-Δ transformation is used to remove the intermediate nodes for simplifying the analysis. After the transformation, R_{1a} and R_{2a} will be removed without affecting the transfer function and R_{1c} and R_{2c} are the shunt resistors at the negative summing node. If assume that $R_{11,13} >> R_{12}$ and $R_{21,23} >> R_{22}$ for keeping the area scaling effects significant, the equivalent resistors values after transformation are given from (1-3) to (1-8):

$$R_{1a} = \frac{R_{11}R_{12} + R_{12}R_{13} + R_{11}R_{13}}{R_{13}} \Rightarrow R_{1a} \approx R_{11} \ , \tag{1- 3}$$

$$R_{2a} = \frac{R_{21}R_{22} + R_{22}R_{23} + R_{21}R_{23}}{R_{23}} \Rightarrow R_{2a} \approx R_{21} \ , \tag{1- 4}$$

$$R_{1c} = \frac{R_{11}R_{12} + R_{12}R_{13} + R_{11}R_{13}}{R_{11}} \Rightarrow R_{1c} \approx R_{13} \ , \tag{1- 5}$$

$$R_{2c} = \frac{R_{21}R_{22} + R_{22}R_{23} + R_{21}R_{23}}{R_{21}} \Rightarrow R_{2c} \approx R_{23} \ , \tag{1- 6}$$

$$R_{1b} = \frac{R_{11}R_{12} + R_{12}R_{13} + R_{11}R_{13}}{R_{12}} \Rightarrow R_{1b} >> R_{1c} , \tag{1- 7}$$

$$R_{2b} = \frac{R_{21}R_{22} + R_{22}R_{23} + R_{21}R_{23}}{R_{22}} \Rightarrow R_{2b} >> R_{2c} . \tag{1- 8}$$

We write the transfer function using conductance for convenience:

$$\frac{V_{out}}{V_{in}} = -\frac{G_{1b}}{G_{2b} + \left(G_{1b} + G_{1c} + G_{2b} + G_{2c}\right) \Big/ A_{ol}} , \tag{1- 9}$$

where, A_{ol} is the open-loop of the opamp, $G_{1,2b}$ and $G_{1,2c}$ are the conductance of the equivalent resistors of $R_{1,2b}$ and $R_{1,2c}$, respectively.

From (1-3) to (1-8), it can be easily shown that the G_{1b} and G_{2b} are much smaller than G_{1c} and G_{2c}. In (1-9), it is obvious that the total conductance $(G_B+G_{Ba}+G_A+G_{Aa})$ will change the ideal transfer function by changing the effective feedback factor β and therefore affect the low frequency performance of the filter as long as the open loop gain A_{ol} is not infinite. Therefore the DC performance will be affected dominantly by G_{1c} and G_{2c}, which are results from the transconductance networks. From the area scaling purpose, the resistors R_{12} and R_{22} should be chosen as small as possible for higher area efficiency. However, R_2 cannot be chosen as an arbitrary value. If R_2 is chosen to be too small, it will require an extremely large A_{ol} to make the $(G_{1c}+G_{2c})/A_{ol}$ be negligible compared with the value of G_{2b}. Through this Y-Δ transform analysis, the feedback factor β has been changed from the single resistor scenario to the trans-resistance network case and this change eventually results a trade off between the resistor area and opamp open loop gain design efforts. If the total equivalent resistance values are fixed for a given time constant of a first order low pass filter, the opamp open loop gain A_{lp} and resistance area are determined by the following equation with a given admissible error γ,

$$\frac{1/a_1R_{12} + 1/a_2R_{22}}{A_{ol}} = \gamma \frac{1}{(a_2+2)a_2R_{22}}. \qquad (1\text{-}10)$$

In (1-10), an attenuation coefficient a, is defined as the ratio of R_{11}/R_{12}, and R_{11} is set to equate to R_{13} in both T-networks. A simple numerical example is shown in Figure 1-4 to show the compromise of resistor size and open loop gain, for different tolerant DC gain error levels (γ=1%, 2%, 5% and 10%) with the assumption that DC loss is 0 dB and the same T-networks are used to replace the input and feedback resistors. Also, the equivalent resistance of transconductance network is assumed to be fixed and it is usually at Meg Ω range when

used in RC active filters in audio frequency range with reasonable monolithic capacitor size. From this example, it is clearly shown that with the unit resistor (R_2) is doubled, the requirement for the open loop gain of the opamp for achieving the same error level decreases by 3 dB and also the total resistors area will increase. If 1% DC gain error is acceptable, the unit resistor should be set bigger than 50 Ω for the reasonable design efforts to obtain 90 dB open loop gain of the opamp.

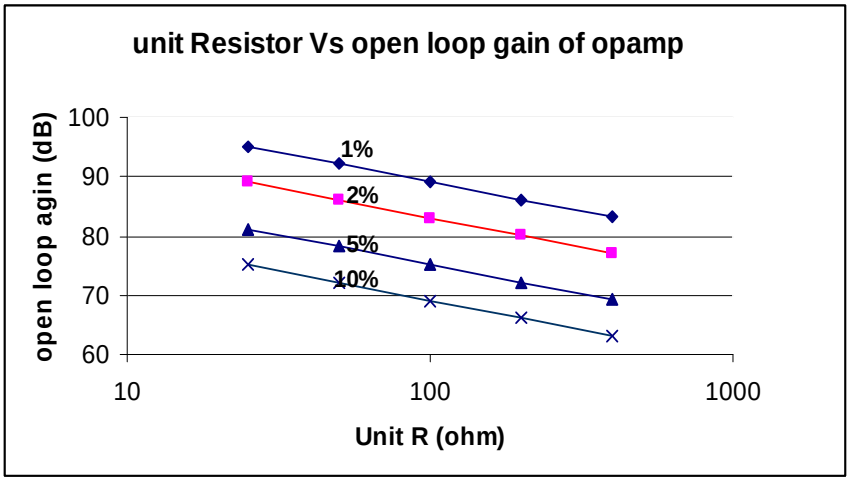

Figure 1- 4-- Open-loop Amplifier Gain Requirements with Changing Unit R at Different Error Tolerance (R_{eq} is fixed as 2 M Ω).

1.3.2 Transconductance Networks and the GB of the Opamp

As discussed in the previous section, the transconductance network will affect the performance of the circuit due to the non-ideality of the opamp. In addition to the finite DC gain of opamp, the frequency dependent gain also will contribute to the error and this will put more stringent requirement of the opamp with the finite gain bandwidth product (GB). Again, a simple first order low pass RC active filter is presented as an example.

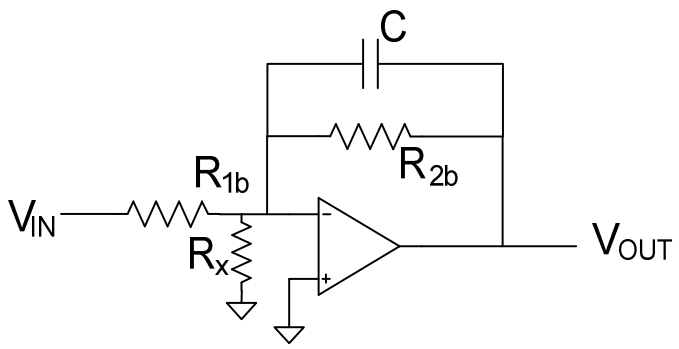

Figure 1- 5-- Equivalent Circuit of the First Order Low-Pass Filter with T-networks.

The same Y-Δ has been done for the circuit in Figure 1-4 and the shunt resistor R_x represents the effective resistance at the negative summing node of opamp. With the same assumption that $R_{11,13} >> R_{12}$ and $R_{21,23} >> R_{22}$, R_x is much smaller than R_1 and R_2. The transfer function was derived including the finite GB in conductance form:

$$\frac{V_o}{V_i} = \frac{-G_1}{sC + G_2 + s/GB\,(sC + G_1 + G_2 + G_x)}. \qquad (1\text{- }11)$$

From (1-11), under the circumstance that $G_x >> G_1$ and G_2, and also be awarded that in monolithic integrated circuit, C/GB is usually very small, the transfer function can be simplified as the first order system:

$$\frac{V_o}{V_i} \approx \frac{-G_1}{s(C + G_x/GB) + G_2}. \qquad (1\text{- }12)$$

In above equation, if *GB* is not big enough to make $G_x/GB << C$, the location of the dominant pole will be shifted. In order to compensate this systematic error due to the transconductance network, either the capacitor size or the GB of the opamp need to be enlarged to make sure that G_X/GB is ignorable compared with *C*. The design should consider the practical capacitor size and compromise it with the GB of the opamp if the admissible error caused by this

conductance need to be tolerated. Since the passive components are vulnerable to the process and temperature variations, RC active filters are used in those applications that have relaxed requirements on the corner frequency without the tuning circuits. So when the value of G_X/GB is less than $x\%$ of the capacitor, the error would be consider to be neglected. Different T-network will result in different G_X and then different trade off between capacitor size and GB of opamp. Assume the same T-networks are used for replacing both R_1 and R_2 and the ratio of $R_{11}/R_{12}=R_{13}/R_{12}=a$. It is easy to derive the equations for effective shunt resistor values and capacitor size from corner frequency requirement as (1-13) and (1-14), where R_{EQ} is the equivalent resistance of T-network and f_{co} is the corner frequency of the filter:

$$G_x = \frac{1}{R_x} = \frac{1}{R_{1c} // R_{2c}} = \frac{2}{(a+2)R_{12}}, \tag{1- 13}$$

$$C \cdot R_{EQ} = 1 \diagup 2\pi f_{co} . \tag{1- 14}$$

Also the relationship between GB and C for compensating the deviation of corner frequency due to the G_x is given:

$$\frac{G_x}{GB} = \frac{x}{100} C . \tag{1- 15}$$

From (1-13), (1-14) and (1-15), the GB can be derived directly from:

$$GB = \frac{x}{100} 4\pi f_{co} a . \tag{1- 16}$$

For a given corner frequency f_{co}, different error budget x will result in different trade off curve between capacitor size and GB of opamp. Figure 1-6 shows the capacitor size with corresponding opamp GB with different values of x (10, 20, 30, 40, 50), assuming f_{co} equates to 5 KHz and R_2 equates to 50 Ω.

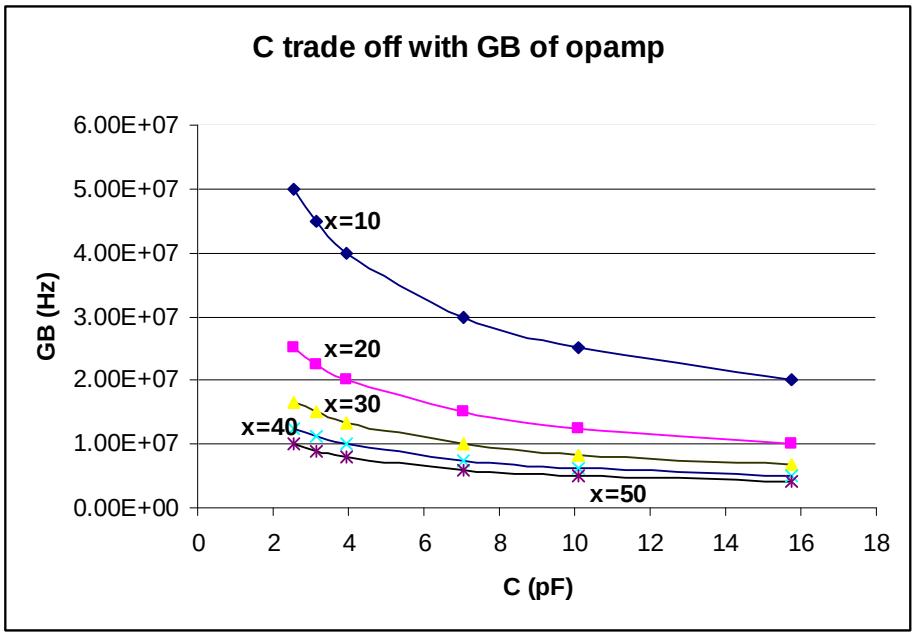

Figure 1- 6 -- Trade-off of the Capacitor Size and GB requirement of Opamp at Different Error Tolerance.

As shown in Figure 1-6, the higher accurate corner frequency requirements, the higher gain bandwidth product is needed. The smaller capacitor size, the faster opamp is needed due to the transconductance networks.

Although above analysis is based on the first order integrator, it is valid for guiding the design with transconductance networks of integrator-based filters and a prototype filter design will be presented in the next section to favorably support those analytical study.

1.4 Third Order Bessel Low Pass Active Analog Filter Design

1.4.1 Filter Topology

A third order Bessel low-pass filter with implementation of those transconductance networks has been designed, including all the consideration discussed above, as shown in

Figure 1-7. The structure of Tow-Thomas biquad [21] followed by a first-order low-pass filter has been adopted. The main reason for choosing this architecture is because all the large value resistors in this topology must be connected to the virtual ground and this satisfies the requirement of the transconductance network that the output end has to be connected to virtual ground to maintain the intended transfer functions. Also this topology exhibits the potential to suppress the distortion due to the large common mode signal with one summing node connecting to virtual ground. The third reason for choosing this topology is that the parasitic capacitance connected to those summing nodes will not cause transfer response detuning effects. Since only passive elements are included in the feedback loop, the second harmonic distortion should be at quite low level and single end configuration is expected to achieve good linearity comparable to those fully differential architectures with other techniques using only active elements.

In order to avoid the distortion caused by the over range of the amplifier linear operation range, the gain of each integrator is set to approximately equate to one.

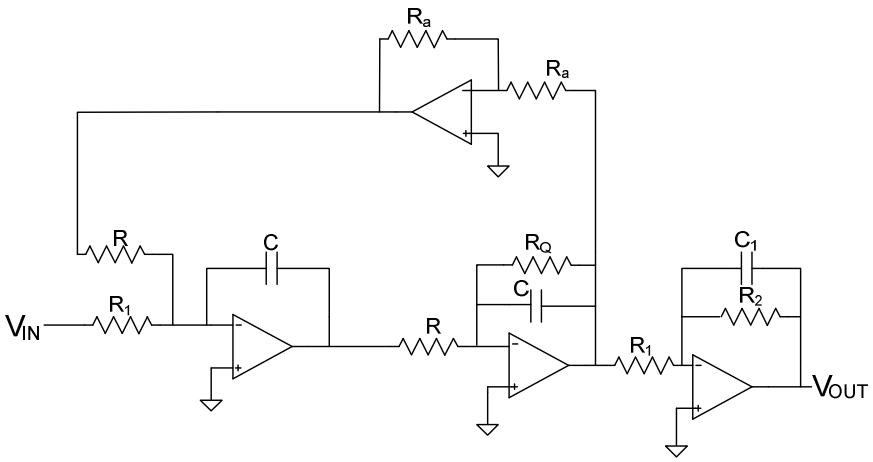

Figure 1- 7 -- Third-Order Bessel Low-Pass Active Filter.

The transfer function is given in (1-17):

$$\frac{V_o}{V_i} = \frac{\frac{R}{R_1}\left(\frac{1}{R^2C^2}\right)}{s^2 + \frac{s}{R_Q C} + \frac{1}{R^2C^2}} \cdot \frac{-1/R_1C_1}{s + 1/R_2C_1} \cdot \tag{1- 17}$$

1.4.2 Passive Elements Design

To determine all the passive elements values, standard Bessel transfer function coefficients are referenced to build the equation sets along with the frequency scale technique for de-normalized the transfer function parameters:

$$\begin{cases} R_Q = \dfrac{1}{a_1\omega_0 C} \\ R = \dfrac{1}{\sqrt{a_0\omega_0^2 C C_1}} \\ R_2 = \dfrac{1}{b_0\omega_0 C} \\ R_1 = \sqrt{\dfrac{1}{a_0 b_0 \omega_0^3 R C^2 C_1}} \end{cases}, \tag{1- 18}$$

where, a_0, b_0, a_1 are standard Bessel transfer function coefficients and are given as: a_0=2.09482, a_1 = 2.095588, and b_0 = 1.32268 [22] while the filter specification is given as w_0=2π×5000, DC loss=0 dB.

The original design space is {R_Q, R_2, R_1, R, C, C_1} and now it is reduced to {R_Q, R_2, R_1, R, C} by setting the capacitor C_1 equates to C for matching performance concern. The design trade off between capacitor and GB of the opamp discussed in previous section play the most important role for determining the capacitor range here. As shown in Figure 1-6, if the error is limited within 20%, the capacitor size should range from 2 pF to 10 pF if

reasonable power is allocate to the opamp for the GB limitation. From this concern, the resistors values will chosen from 2 Meg Ω to 10 Meg Ω.

1.4.3 Passive Elements Area Optimization

Because RC active filter is very attractive for its high linearity and now is practical by implementing the transconductance networks, issues of the further reduction of the total passive area would be interesting. Some work has been reported for the optimization of total passive area and it has been proved in close form that optimum passive area would be achieved when the total resistor area are equal to the total capacitor area under the constrains of the fixed corner frequency and DC gain [22] and this topic will be discussed in the later section. Several popular architectures including the first order integrator, first order integrator with transconductance network, Tow-Thomas Biquad w/o transconductance networks and bridge T feedback circuit have been studied and all have been proved to hold this conjecture. Another function could be set according to this theorem. The process parameters about the sheet resistance and sheet capacitance can be set as R_d and C_d, respectively,

$$\frac{2R + 2R_1 + R_2 + R_Q}{R_d} = \frac{3C}{C_d}. \qquad (1\text{-}19)$$

Combining the equation set (1-18) and equation (1-19), it can be solved for all the passive components' values. When calculating the coefficient R_d, multiple contacts would be expected for reducing the total contact resistance and this would lead to a width of the Poly resistor be little larger than the minimum value. In those equations, all the resistors R, R_1, R_2 and R_Q will be replaced by transconductance T-network as shown in Figure 1-8.

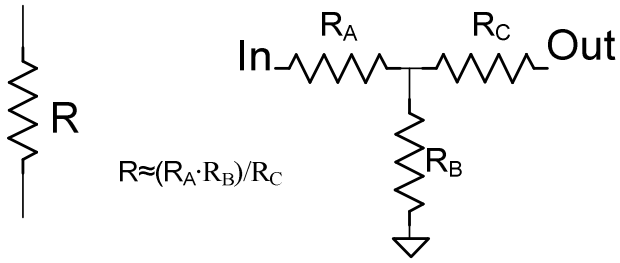

Figure 1- 8 -- Transconductance Network Used to Replace All the Single Resistors.

The common central layout technique is used to implement the Polysilicon resistors in order to obtain satisfied match performance so as reasonable corner frequency accuracy. For this reason, the transconductance networks have been modified slightly from the format in analysis above. Resistor R_A and R_B are chosen to be 10 K Ω, and 50 Ω, respectively for all the transconductance networks and *Rc* is determined by:

$$R_C \cong \frac{R_{design}}{R_A / R_B} . \qquad (1\text{- }20)$$

where R_{design} is the nominal values for each resistor. The reason for choosing 50 Ω for R_B is that any smaller resistor would result even smaller passive area but would also demand open loop gain to be higher than 93 dB for 1% error tolerance and this can be clearly shown in Figure 4. All the nominal passive components values are listed below.

C= 3.5 pF

R_{QN}= 4.339 M Ω,

R_N = 6.284 M Ω

R_{1N}= 6.573 M Ω

R_{2N}= 6.876 M Ω.

This set of passive elements values satisfied all above considerations: Standard Bessel low pass transfer function; realistically op amp open loop gain and GB design efforts;

optimum passive elements allocations and the approximately unit gain for each integrator stage.

1.4.4 Op Amp Design

The op amps used in this application needed to be high performance so as not to degrade the filter operation noticeably along with the transconductance networks. In order to attain the high linear performance as standard RC active filters, the following features were specified:

- ability to drive loads of the order of 10 k Ω resistor and 20 pF capacitor;
- THD > 90 dB, when configured with feedback;
- linear output voltage range = 2 V p-p;
- open loop gain > 90 dB;
- gain bandwidth produce >50 MHz;
- PM > 70 degree at unit gain frequency.

A two-stage telescope cascode configuration meeting above specifications was chosen as shown in Figure 1-9. The input stage is a telescope cascode stage which provides high gain and the second stage is a class-A common-source stage, exhibiting high linearity and large output swing. The quiescent current is high in the output device (M_9) to provide necessary high frequency pole to achieve enough unit gain frequency. The over drive voltages of input devices of both stages (M_1 and M_{10}) were carefully chosen to achieve good settling performance. The zero-pole cancellation compensating technique was used for stabilizing this two-stage amplifier because it is more efficient than the single miller capacitor compensation with cancellation of the right half plane zero. Simulation showed this

amplifier can achieve 103 dB DC gain, 60 MHz gain-bandwidth product with 70 degree phase margin with total power 20 *mW* at 5 V power supply.

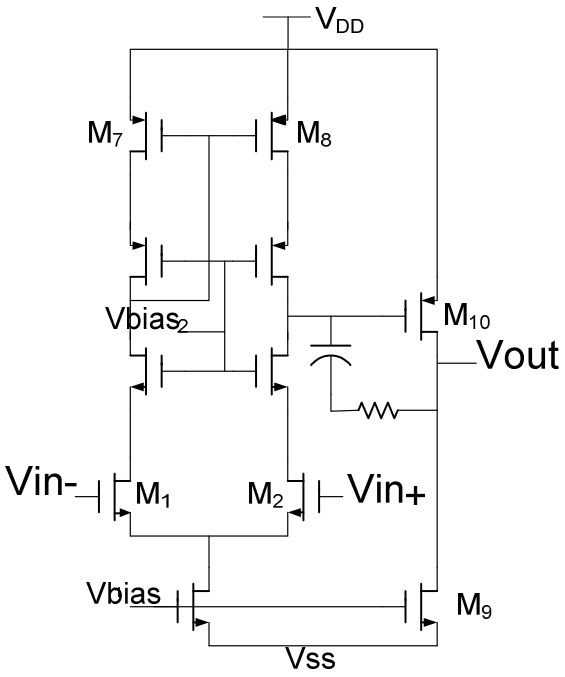

Figure 1- 9 -- Simplified Two Stage Op Amp Design.

1.5 Experimental Results

The prototype filter was fabricated using AMI05 0.6 um double polysilicon standard CMOS process with 5 V power supply. The total die area is 0.40mm^2 and the area per pole is 0.13 mm^2 including 0.05 mm^2 for capacitors, 0.05 mm^2 for resistors and 0.25 mm^2 for 4 op amps. The active die area microphotograph is shown in Figure 1-10. The test is operated at room temperature from a nominal 5 V supply.

The experimental results exhibit good agreement with the predicted results from the simulations. The filter's frequency response is shown in Figure 1-11 and it matches with the designed cut-off frequency very well. The average cut off frequency from 5 fabricated chips

is 5.5 KHz, which is 10% variation from the designed value and this result also showed a favorably support to our analysis for the frequency deviation due to the transconductance networks. Pass band loss is 0.9 dB which is little lower than the simulation results, 0.2 dB, and this is due to process variations of the poly resistors. The stop band rejection is lower than 62 dB and this measurement is limited by the noise level of the test device.

The linearity performance has been testified using a spectrum analyzer: HP 3585A, and the result is shown in Figure 1-12. The input voltage is locked at 2V peak-to-peak with pass-band frequency at 716 Hz. This experimental results shows a close results from the previous simulation results, 2^{nd} harmonic distortion at around -70 dB level and the 3^{rd} harmonic is little higher than simulation results and the reason for this deterioration is possible due to the capacitor nonlinearity and the cross-coupled capacitor structure [16] will further surprise it. Shown in Figure 1-13, SFDR has been plot with different pass-band input frequencies. Form this figure, it is clearly shown that SFDR remain the same level with the input signal frequency sweep and incased when input signal beyond 2000 Hz range. This improved SFDR is due to the higher harmonics was getting into stop band when input signal close to corner frequency and have be attenuated by the frequency shaping of the low pass filter.

It is noticed that the whole filter linearity is worse than op amp linearity in feedback configuration and this is mainly because of the transconductance network changed the effective feedback factor and therefore reduced total loop-gain. The detail analysis of this phenomenon will not be discussed further in this section but will be included in extended work. Another dynamic range optimization technique [13] [24] may be used to further improved the dynamic range.

The noise is about 5.6 uV/√Hz up to 5 KHz and total noise at the low frequency band is dominant by 1/f noise. This noise level can be lower by incasing the input transistor size and of course with sacrifice some die area.

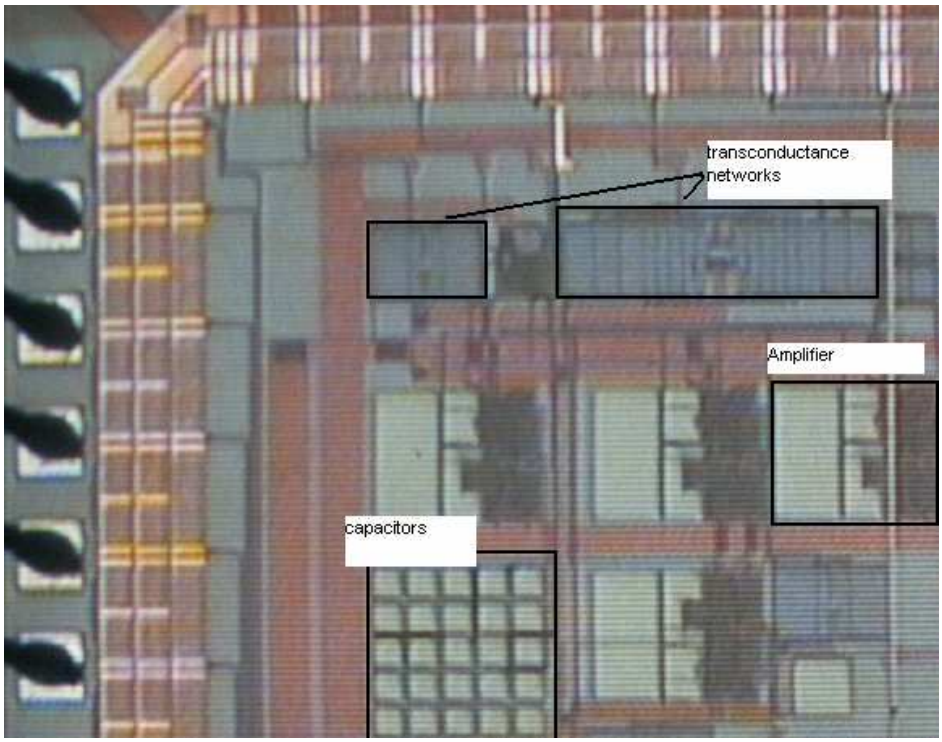

Figure 1- 10 -- Microphotograph of the Active Die Area

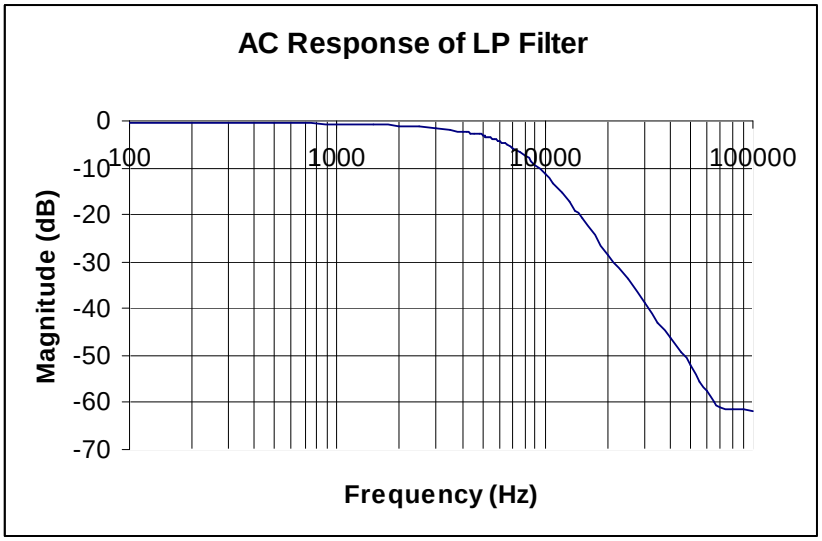

Figure 1- 11 -- Measured Frequency Response

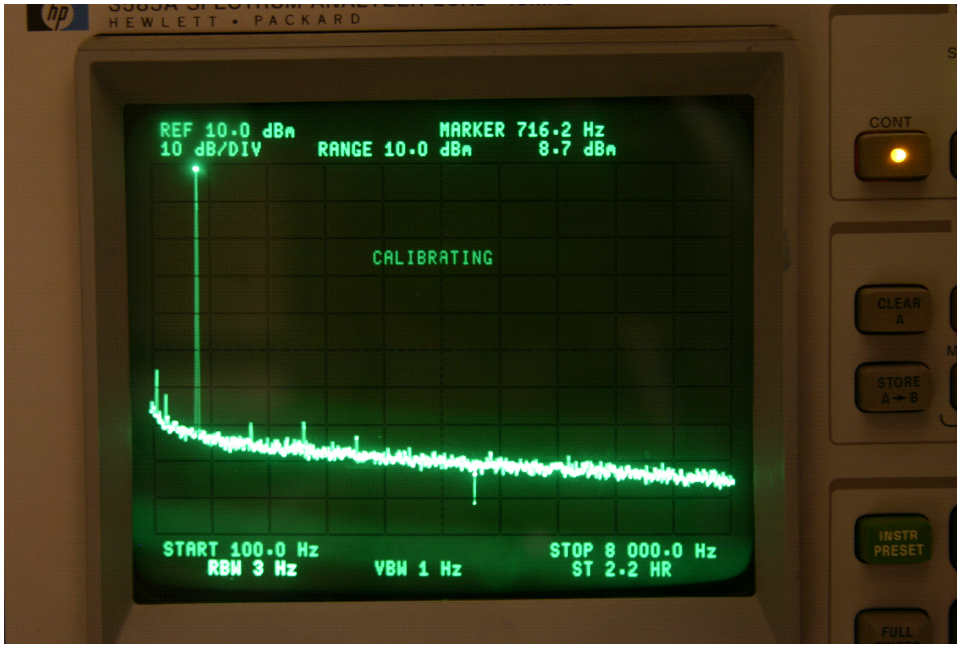

Figure 1- 12 -- Measured Spectrum Performance

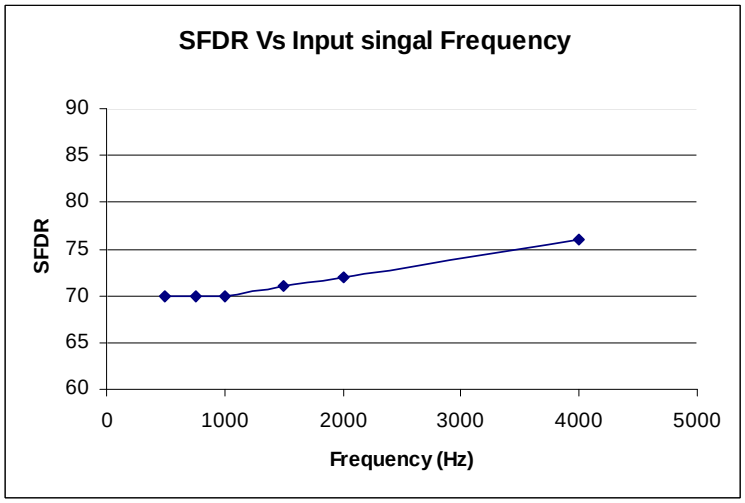

Figure 1- 13 -- Measured SFDR With Input Frequency.

The summary of the prototype filter measurements is tabulated in Table 1-3.

Table1- 3 Summary of the Experimental Results of the Prototype Filter

Filter Type	3rd-order Bessel Low-pass
Technology	0.5 μm double-poly CMOS
Active die area	0.4 mm^2
Supply Voltage	5 V
Current Consumption	16 mA
Cut-off Frequency	5.5 KHz (10% variation)
DC loss	0.9 dB
Pass-band deviation	0.1 dB
Stop-band rejection	62 dB
SFDR ($2V_{pp,}$ 716 Hz)	70 dB

1.6 Conclusion

A method of implementing a highly linear continuous-time filter for low frequency applications in CMOS has been proposed. A simple transconductance network replaced the large value resistors in the active RC filters in audio frequency range. The analysis of the transconductance network's effect related to the non-ideal opamp is the main challenge in this technique. A systematic study of this relationship provides a practical design strategy for adopting the proper transconductance networks so that the area associated with passive components will be dramatically reduced and high-linearity is maintained. The experimental results show a promising THD performance and frequency response, which are among the best linearity performance ever being reported. The prototype filter displays the feasibility of this technique in low frequency applications with slightly increased amplifier design efforts.

1.7 References

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CHAPTER 2 TRANSCONDUCTANCE NETWORK STUDY IN HIGH LINEAR CIRCUITS

2.1 Introduction

Resistors are widely used in circuits implemented at the printed circuit board level but the practical implementation of resistors in standard high-volume CMOS processes is limited because of the area required for the physical implementation of the resistors. In today's popular CMOS processes, polysilicon (with silicide blocking) is the only feature that is consistently available that can produce resistors with attractive voltage coefficients, reasonable matching properties, and reasonable process variability. Since the sheet resistance of polysilicon in such processes is rather low (typically between 10 Ω/□ and 50 Ω/□), the area required for resistors beyond a few KΩ is very large [1] and the power required to drive small resistors at reasonable signal levels is high and it is these two factors that dominantly limit the practical implementation of resistors in such processes. Although this limitation is of concern in essentially all circuits where resistors would offer attractive circuit potential, it is of particular concern when building active filters that operate from the audio frequency range up to the MHz range and beyond since the long time constants inherently require either large valued resistors or large capacitors. Some well-established techniques have been reported to work around this problem. One of the most popular traditional solutions for continuous-time filters are the MOSFET-C filters [1]-[5], in which a MOS transistor operating in the triode region replaces the passive resistor and this structure is easy to implement with operational amplifier while maintaining (what of) traditional active RC filters. Another well established technique is g_m-C filters [6]-[10]. However, there is few published approaches can solve the

linearity with active transconductance cell reported in [1]-[10] and they can only achieve THD of about 40~60 dB. Therefore, the solution for manage the total area of passive resistors with high linearity is of particular interested in low distortion circuit implementations.

Although the two-terminal standard resistors are of particular interested, those resistors sometimes are more often used as the transconductance device with an attractive low voltage coefficient, which mean it provides high linear transfer relationship between the input voltage and output current.

Several authors [11]-[14] have discussed the use of various passive ladder-type resistor networks comprised of relative low-valued resistors for the implementation of the transconductance elements. In Chapter 1, experimental results also proved that by using the transconductance network, a high linear analog filter can be realized within very limited die area. And the relationship between the transconductance network and the amplifier design has been discussed in Chapter 1. In this Chapter, the relationship between the transconductance with more general circuit characteristics such as the total passive area, linearity, noise performance, and process variations will be exploited in the following sections. Experimental results will be presented with the discrete circuits as approves of the all the analytical works. In the last section, the issue about the mapping between the design space and performance space will be addressed.

2.2 Area Efficiency Study

The purpose to use the transconductance networks is to reduce the passive component areas so that the high linear material, polysilicon, can be used in today's high volume standard CMOS processes. The question about the area efficient naturally rises with this

approach. It is considerably important to know exactly the efficient of saving the die area by using the transconductance network.

The discussion will focus on two very popular transconductance structures shown in Figure 2-1. The first is a generalization of what some authors term a T- feedback network [11]. If the network is reduced to a single stage, this transconductance network is comprised simply of a single resistor R_S so when applied in the amplifier circuit of Figure 1-1(b), it is equivalent to the feedback structure of Figure 1-1(a). When a two-stage structure is used it becomes the popular T network. Generally R_P is considerably less than R_S when using the T-network to increase the overall transresistance, the reverse value of the transconductance network. The circuit of Figure 2-1(b) is recognized as an n-stage R-2R network. It was used recently by Ismail [13] and Rijins [14] for obtaining an area-efficient programmable transresistance for a filter and VGA applications and is shown in the highest transresistance configuration in Figure 2-1(b). The left-most 2R resistor does not contribute to the largest transresistance but was included in [13] to provide for the binary programmability of the transresistance.

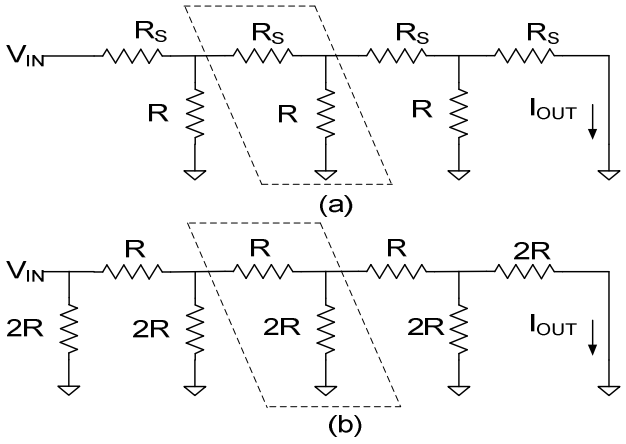

Figure 2- 1 -- Ladder-Based Transconductor a) 4-Stage T-network, b) 4-Stage R-2R network.

In both cases the basic element that is repeated to increase the number of stages is shown in the dashed box. The distinction between the T-network and the R-2R network is only in how the component values are selected.

It will be assumed that the width of all resistors is fixed and that a reference resistor with this width is identified. This reference resistor can be considered as a unit resistor. It will also be assumed that all resistors are realized with a series connection of the appropriate number of unit resistors. This reference will be of minimum width if the goal is to minimize the total resistor area. In Figure 2-1, it is assumed that the reference resistor is the resistor designated as "*R*" and that the nominal area of this reference resistor is given by A_{RN}. It thus follows that the area for a resistor R_X is given by:

$$A_{RXN} = A_{RN} \frac{R_{XN}}{R_N}, \tag{2- 1}$$

where R_{XN} is the nominal value for the resistor R_X and R_N is the nominal value for the reference resistor R.

For notational convenience a reference resistor scaling factor θ of a transresistance network has been defined as the ratio of the nominal equivalent transresistance, $R_{EQN,}$ to the nominal resistance of the reference resistor. Formally, it is clearly that θ can be derived:

$$\theta = \frac{R_{EQN}}{R_N}. \tag{2- 2}$$

For R-2R structure, it is well known that the total equivalent transconductance is given by a single expression shown below:

$$R_{R-2R}(n) = 2^n R, \tag{2- 3}$$

where, n denotes the total number of stages. It is clearly shown that the overall transconductance increases with the power of 2 and large value then can be achieved by choosing a large number of *n*. Follows from (2-2) and (2-3), the resistor scaling factor of R-2R network is given:

$$\theta_{R2R} = 2^n. \tag{2- 4}$$

For the general T-network, the expressions of the total equivalent resistance are not unique and they are the function of the number of stage *n*:

$$R_T = \begin{cases} aR & n=1 \\ (2+a)aR & n=2 \\ (2+a)^2 aR & n=3 \\ \left[(2+a)^3 - 2(2+a)\right]aR & n=4 \\ [(a+2)^4 - 3(a+2)^2 + 1]aR & n=5 \\ [(a+2)^5 - 4(a+2)^3 + 3(a+2)]aR & n=6 \\ [(a+2)^6 - 5(a+2)^4 + 6(a+2)^2 - 1]aR & n=7 \\ [(a+2)^7 - 6(a+2)^5 + 10(a+2)^3 - \\ \quad 4(a+2)]aR & n=8 \end{cases}. \tag{2- 5}$$

It is assumed that in a certain general T-network, an identical ratio of series resistor, R_s, over parallel resistor, R_p, has been used and this ratio is nominated as *a*. For general T-network, the equivalent resistance is proportional to $(2+a)^{n-1}$ and real large value can be obtained with even moderate large values of *a* and *n*. A parametric closed-form expression for the reference resistor scaling factor for the T-network appears to be somewhat complicated but θ_T for any fixed *n* and *a* can be obtained directly from (2-5) by simply dividing the terms on the right hand side by R. Table 2-1 exhibits a comparison of the transresistance of the R-2R

network and the T-network with a =4, 10, and 25. With a=10 and 3 stages only, the equivalent resistance of the T-network increases by over 3 orders of magnitude and with a=25 and n=8, the transresistance of the T-network increases by over 11 orders of magnitude. Although the increase in the transresistance of the R-2R network is geometric, it is much smaller than that obtainable for the general T-network when the value of a is even modestly large.

In the next part, the study will focus on the area efficiency, in another word, how efficient those two structures to realize large value of equivalent resistance associate with the same limited area and this problem is probably more of concern in the practical design works. We will define the resistance area efficiency, η, to be the ratio of the transresistance, R_{EQ}, to the total resistance of the network. Formally, it is given as:

$$\eta = \frac{R_{EQ}}{R_{TOT}}. \tag{2- 6}$$

In (2-6), η represents an area savings factor for using a transresistance network rather than a single resistor for implementing a given transresistance. For the R-2R network, it is easily to find that the total resistance is $R_{TOT}=(3n+4)R$ so that the area efficiency is given by the expression:

$$\eta_{R-2R}(n) = \frac{2^n}{3n+4}. \tag{2- 7}$$

For the general T-network, the total resistors used for n stage with fixed value a is given as:

$$R_{TOT} = (n \cdot a + n - 1)R. \tag{2- 8}$$

Combining (2-5) and (2-8), the area saving factor of T-network is readily obtained as below:

$$\eta_T = \begin{cases} \dfrac{a}{na+n-1} & n=1 \\ \dfrac{(2+a)a}{na+n-1} & n=2 \\ \dfrac{(2+a)^2 a}{na+n-1} & n=3 \\ \dfrac{\left[(2+a)^3-2(2+a)\right]a}{na+n-1} & n=4 \\ \dfrac{\left[(a+2)^4-3(a+2)^2+1\right]a}{na+n-1} & n=5 \\ \dfrac{\left[(a+2)^5-4(a+2)^3+3(a+2)\right]a}{na+n-1} & n=6 \\ \dfrac{\left[(a+2)^6-5(a+2)^4+6(a+2)^2-1\right]a}{na+n-1} & n=7 \\ \dfrac{\left[(a+2)^7-6(a+2)^5+10(a+2)^3-4(a+2)\right]a}{na+n-1} & n=8 \end{cases}. \quad (2\text{-}9)$$

Again, numerical example is useful to shown how that much higher area efficient this T-network can achieve with certain realistic values of *n* and *a* compared to the R-2R network. For example, the area efficiency can only larger than 1 when the 5 or more number of stages structure being used and it takes 8 stages to improve the area efficiency to 10. On the contrary, T-network offers much higher efficiency for even relatively small values of *a* and *n* and it will be extremely area efficient with increasing values of *a* and *n*: η will be over 9 decades with 8 stage T-networks and an equals to 25. The comparison of area efficiency is also tabulated in Table 2-1.

Table 2- 1 Equivalent Transconductance and Area Efficiency of Transconductance Networks

$R_{EQ,}\theta$					Area Efficiency, η			
n	R2R	T (a=)			R2R	T (a=)		
		4	10	25		4	10	25
1	2	4	10	25	0.3	1	1	1
2	4	24	120	675	0.4	2.67	5.71	13.2
3	8	144	1440	1.82E+04	0.6	10.3	45	236.7
4	16	816	1.70E+04	4.91E+05	1	42.9	396	4764
5	32	4760	2.03E+05	1.32E+07	1.7	198	3760	1.03E+05
6	64	2.77E+04	2.42E+06	3.57E+08	2.9	956	3.72E+04	2.30E+06
7	128	1.62E+05	2.88E+07	9.63E+09	5.1	4750	3.79E+05	5.31E+07
8	256	9.42E+05	3.44E+08	2.59E+11	9.1	2.41E+04	3.95E+06	1.25E+09

2.3 Linearity with Transconductance Networks

In the previous section, it has been proved that high area efficiency can be obtained by choosing proper general T-networks and thus the area issue limiting the implementation of passive resistors seems to be solved. It will be very promising to use those passive components with this technique since the high linearity will be achieved without any other circuitry design. Therefore, the key issue is to maintain the high linearity with the total area dramatically reduced. In the practical design process, it is interested to reveal the factor that the harmonic levels of the simple resistor feedback amplifier circuit will change along with different T-networks comprised of different values of R_s and R_p. The simulation shows that the harmonics distortions will not, nevertheless, change if ideal amplifier has been used. This implies that the transconductance networks will change the circuit linearity characteristics and thus modify the distortions level which are generated mainly by the operational amplifiers.

In the following par, it will be presented that the transconductance network will change the feedback factor β. It is well known that the single resistor feedback amplifier as shown in Figure 2-2 has the feedback factor as given in (2-10).

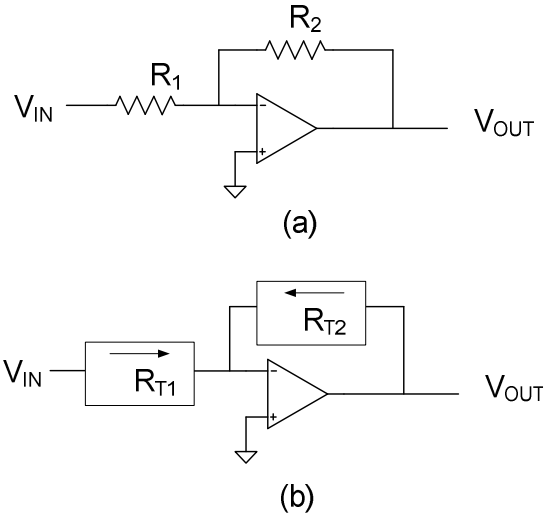

Figure 2- 2 -- Resistor Feedback Amplifier.

$$\beta = \frac{R_1}{R_1 + R_2}. \qquad (2\text{-}10)$$

After the single resistors have been replaced by T-networks, the circuitry is further undergoing with Y-Δ transform for more convenient analysis.

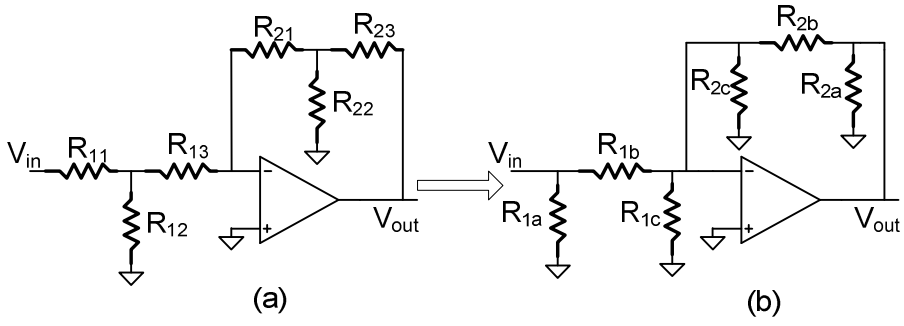

Figure 2- 3 -- T-network Feedback Amplifier with Y-Δ transform.

With the reasonable value of R_{11}/R_{12} and R_{13}/R_{12} for efficiently use of passive component area, the equivalent input port resistors values after Y-Δ transformation are given as (2-11)-(2-13):

$$R_{1a} = \frac{R_{11}R_{12} + R_{12}R_{13} + R_{11}R_{13}}{R_{13}} \Rightarrow R_{1a} \approx R_{11}\,(R_{11} >> R_{12}\ R_{13} >> R_{12})\,, \tag{2- 11}$$

$$R_{1c} = \frac{R_{11}R_{12} + R_{12}R_{13} + R_{11}R_{13}}{R_{11}} \Rightarrow R_{1c} \approx R_{13}\,(R_{11} >> R_{12}\ R_{13} >> R_{12})\,, \tag{2- 12}$$

$$R_{1b} = \frac{R_{11}R_{12} + R_{12}R_{13} + R_{11}R_{13}}{R_{12}} \Rightarrow R_{1b} = R_{11} + R_{13} + \frac{R_{11}R_{13}}{R_{12}} = \left(1 + \frac{R_{11}}{R_{12}}\right)R_{13} + R_{11}\,. \tag{2- 13}$$

It is very clearly to show that R_{1a} and R_{1c} are significantly smaller than R_{1b} with the assumptions of original T-networks. And the circuit will be simplified further as shown below:

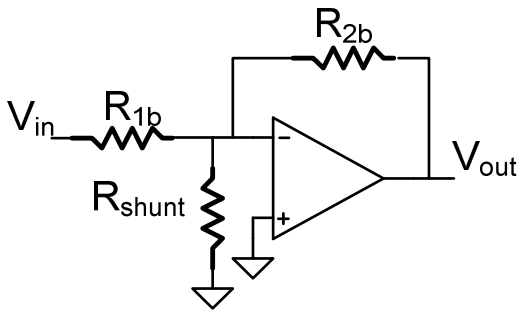

Figure 2- 4 -- Simplified Equivalent T-network Feedback Amplifier

In Figure 2-4, R_{shunt} represent the parallel combination of R_{1c} and R_{2c} and as discussed previously, R_{shunt} is much smaller than R_{1b} and R_{2b} if moderate large value chosen for R_s/R_p in T-network for achieving high area efficiency. One can easily derive the feedback factor as:

$$\beta_T = \frac{R_{1b}R_{shunt}}{R_{1b}R_{shunt} + R_{2b}R_{shunt} + R_{1b}R_{2b}}\,. \tag{2- 14}$$

Obviously, this feedback factor is smaller than the single resistor feedback amplifier given in (2-10). For multiple numbers T-network, the same analysis procedure could be repeated and the circuit is finally simplified as the same format as shown in Figure 2-4. Therefore, β is a function of the number of stage, *n*, and the ratio of R_s/R_p, represented as *a*. This two dimensional equation can be described in Figure 2-5.

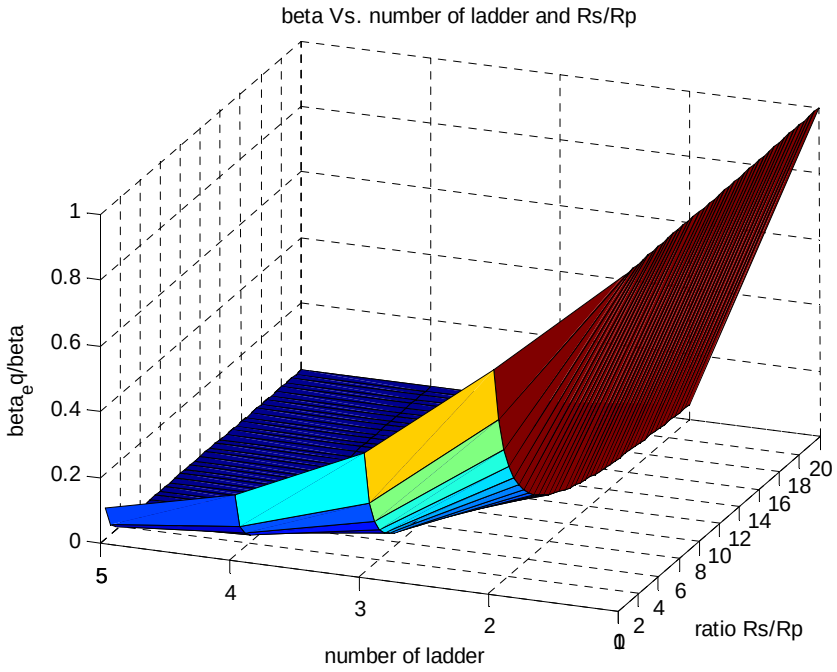

Figure 2- 5 -- β_T/β Vs the number of stage and R_s/R_p.

The equivalent feedback factor β_T reduce significantly with the increasing number of stage and larger ratio of R_s over R_p. After the number of stage being increased over 3, with even moderate ratio of R_s over R_p, the equivalent feedback factor is only 1%-10% of the value with single resistor feedback circuit. Thus the higher area efficient the T-network offers, the lower overall feedback factor of the circuit. According to [16], the relationship between the feedback factor β and the second order harmonic distortion is briefly presented below. The general feedback circuit model is shown in Figure 2-6.

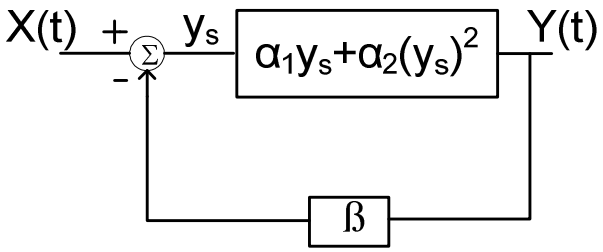

Figure 2- 6 -- General Feedback System Block Diagram.

In Figure 2-6, the input signal is assumed to be comprised of the fundamental and the second order harmonic distortion: $x(t) = A_1\cos(wt) + A_2\cos(2wt)$, and the amplifier is modeled as the linear part plus the second order component: $\alpha_1 x(t) + \alpha_2 x(t)^2$. Also assume the output *y(t)* comprised of the fundamental and second order harmonics and the coeffieicents are *a* and *b*, respectively. It is clearly to derive:

$$\begin{aligned} ys &= x(t) - \beta y(t) \\ &= A_1\cos(\omega t) + A_2\cos(2\omega t) - \beta\left[a\cos(\omega t) + b\cos(2\omega t)\right], \end{aligned} \tag{2- 15}$$

$$\begin{aligned} y(t) &= \alpha_1(y_s) + \alpha_2(y_s)^2 \\ &= \alpha_1(A_1 - \beta a)\cos(\omega t) + \alpha_1(A_2 - \beta b)\cos(2\omega t) + \alpha_2\cdot\frac{1}{2}\cdot(A_1 - \beta a)^2\left[\cos(2\omega t) + 1\right]. \\ &+ \alpha_2(A_2 - \beta b)^2\cos^2(2\omega t) + 2\alpha_2(A_1 - \beta a)(A_2 - \beta b)\frac{1}{2}\left[\cos(3\omega t) + \cos(\omega t)\right] \end{aligned} \tag{2- 16}$$

After the each frequency component coefficient being sorted, the expression of *a* and *b* can be derived as:

$$a = \alpha_1(A_1 - \beta a) + \alpha_2(A_1 - \beta a)(A_2 - \beta b), \tag{2- 17}$$

$$b = \alpha_1(A_2 - \beta b) + \frac{1}{2}\alpha_2\cdot(A_1 - \beta a)^2. \tag{2- 18}$$

Solving above two equations for *a* and *b* with ignoring the coefficients α_2 since it is usually significantly smaller than α_1, the fundamental and second order harmonic distortions coefficients are give by:

$$a \cong \frac{A_1\alpha_1}{1+\beta\alpha_1}, \tag{2- 19}$$

$$b \cong \frac{\alpha_1 A_2 + \frac{1}{2}\alpha_2 A_1^2}{(1+\alpha_1\beta)^3}. \tag{2- 20}$$

Thus the harmonic distortion due to the second order nonlinearity would be derive from (2-19) and (2-20) as:

$$\frac{b}{a} = \frac{\alpha_1 A_2 + 0.5\alpha_2 A_1^2}{A_1\alpha_1(1+\beta\alpha_1)^2}, \tag{2- 21}$$

If (2-21) is further simplified with the assumption that good signal sources with quite small value of A_2 has been used, the ratio of the second harmonic distortion over the fundamental is shown as:

$$\frac{b}{a} \cong \frac{1}{2}\frac{\alpha_2}{\alpha_1} A_1 \frac{1}{(1+\alpha_1\beta)^2}, \tag{2- 22}$$

From (2-22), we can see that the distoriton level will incrase if the feedback factor β has been reduced and all other circuit coefficients are remian unchanged. Also if assume the amplifier has significantly larger linear coeffieicent α_1, than the second order harminc coeffieicnt α_2, (2-22) can be modified as:

$$\frac{b}{a} \cong \frac{1}{2}\frac{\alpha_2}{\alpha_1}\frac{A_1}{(\alpha_1\beta)^2}. \tag{2- 23}$$

From (2-23), approximately say, the second harmonic will be proportional to the reverse of β^2 and it will rise about 12 dB with β reduce by half. However, the circuit shown in Figure 2-2 is different from the general feedback block diagram shown in Figure 2-6. The experssion of the negative input node V_- derived from Figure 2-2 is expressed as:

$$V_- = V_{in}\left(\frac{R_2}{R_1+R_2}\right)+V_{out}\left(\frac{R_1}{R_1+R_2}\right). \qquad (2\text{-}24)$$

And the modified the general models is shown:

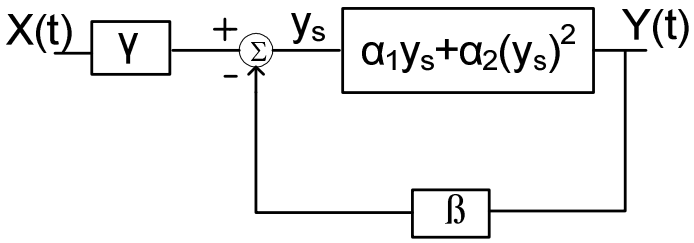

Figure 2- 7 -- General Feedback Block Diagram of Figure 2-2 (a).

In Figure 2-7, the feedback β and the input coefficient γ are given as:

$$\beta = \frac{R_1}{R_1+R_2}, \qquad (2\text{-}25)$$

$$\gamma = \frac{R_1}{R_1+R_2}. \qquad (2\text{-}26)$$

The same analysis procedure of (2-15)-(2-18) have been repeated and the fundamental coefficient, the second harmonic coefficient, and the ratio between those two are then given by (2-27)-(2-29), respetively:

$$a \cong \frac{A_1\gamma\alpha_1}{1+\beta\alpha_1}, \qquad (2\text{-}27)$$

$$b \cong \frac{\alpha_1 A_2 \gamma + \frac{1}{2}\alpha_2 A_1^2 \gamma^2}{(1+\alpha_1\beta)^3}, \tag{2- 28}$$

$$\frac{b}{a} \cong \frac{1}{2}\frac{\alpha_2}{\alpha_1} A_1 \frac{\gamma}{(1+\alpha_1\beta)^2} \cong \frac{1}{2}\frac{\alpha_2}{\alpha_1}\frac{A_1 \cdot \gamma}{(\alpha_1\beta)^2}. \tag{2- 29}$$

For the sepcific circuit shown in Fig2-3, in which, the T-network replaced the single resistor to realize resistor feedback amplifier, if the unit gain is required, the γ is given:

$$\gamma_T = \frac{R_{2b}R_{shunt}}{R_{1b}R_{shunt} + R_{2b}R_{shunt} + R_{1b}R_{2b}}. \tag{2- 30}$$

So γ_T shares the same value as β_T if the symmetrical T-networks are used in Figure 2-3, in which case, R_{1b} equals to R_{2b}. If the different T-networks are applied to the same circuit which only changed the feedback factor β and input coefficient γ and left other circuit coefficents unchanged, such as A_1, A_2, α_1 and α_2, the second harmonic distorion associated with the amplifier given in (2-29) will be proportional to the reverse of β and it will rise roughly about 6 dB with every half reduction of β.

Experimental results will be shown in the following part to verify the close form analytical conclusions. Simple discrete time circuits has been built up according to the Figure 2-3 and the operaitonal amplifier is chosen AD8032A from Analog Devices Inc. Spectrum analyzer, HP 3585A, has been used to verify the harmonic distortion level. For the first set of testing, simple single T-network have been used with different values of series resistors and parallel resistors and the overall equivalent transconductance has been remaind the same. Because it is very hard to estimate the distoriton level without knowing the exact values of α_1 and α_2, the second harmonic distortion level with single resistor has been used as the reference point and the linearity degradation due to the different transconductance networks

resulted from both analytical equations and spectrum analyzer are compared in the Figure 2-8.

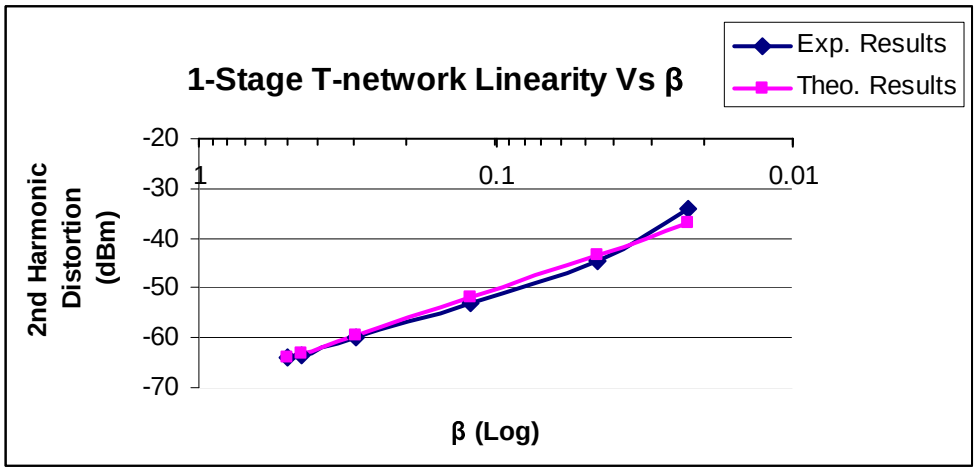

Figure 2- 8 -- Linearity Degrade Vs β Change of 1-stage T-network.

It is clearly shown that the experimental results match the analytical predictions very well except for the smallest value of β. As addressed in [15], the change of β also influent the low frequency gain and frequency response of the amplifier. When β approaching to really small value, the frequency response is also deteriorated so that the second harmonic distortion level is even worse than what (2-29) predict. This difference between the theoretical prediction and measurements is more obviously in the follow figure, in which 2-stage T-networks are used with more aggressive reduced β values.

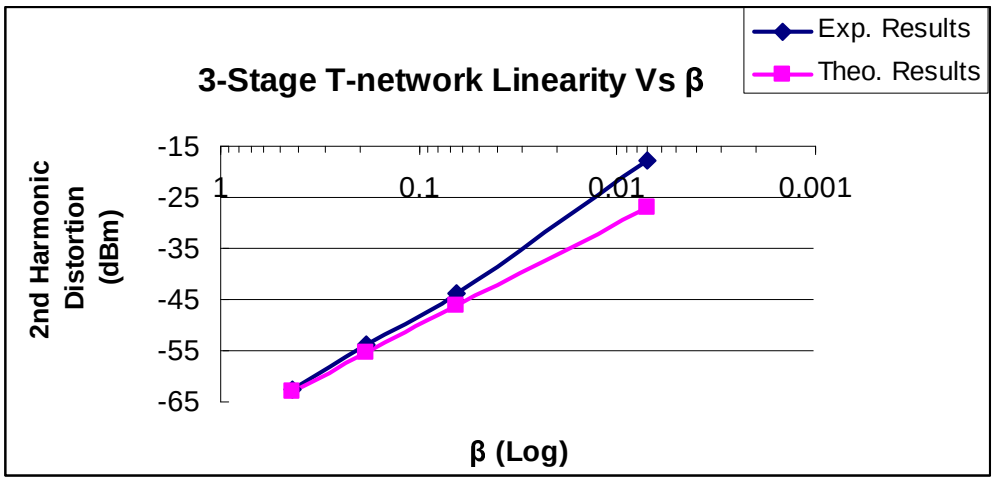

Figure 2- 9 -- Linearity Degrade Vs β Change of 2-stage T-network.

Figure 2-8 and 2-9 verify the theoretical analysis and demonstrate the trade off between the linearity and feedback β. Because the higher area efficiency achieved, the smaller β resulted, the trade off is actually between the area efficiency and linearity with implementation of transconductance networks.

2.4 Transconductance Networks and Noise Performance

In the previous section, the relationship between the linearity and feedback factor β has been discussed. The next very important circuit characteristic is the noise performance. Noise level is the major fundamental limitation of the performance for almost all the electrical circuits and for some system, such as communications system, noise is a more important concern. So understanding the relationship between the transconductance networks and noise is of particular interested and will be presented in the following paragraph.

At first, only the thermal noise from the passive components is taken into consideration. The simple resistor feedback amplifier noise model is shown in Figure 2-10.

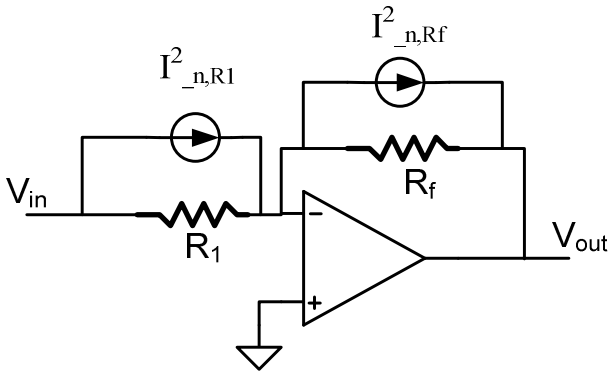

Figure 2- 10 -- Noise Model of Simple Resistor Feedback Amplifier.

It is straightforward to derive the total output noise due to those two resistors:

$$V_{ntot}^2 = \left(I_{nR1}^2 + I_{nRf}^2\right)\cdot R_f^2 = 4KT\left(\frac{R_f^2}{R_1} + R_f\right), \qquad (2\text{- }31)$$

Then the single-stage T-networks are used to replace the single resistors R_1 and R_f and the noise model is now shown in Figure 2-11.

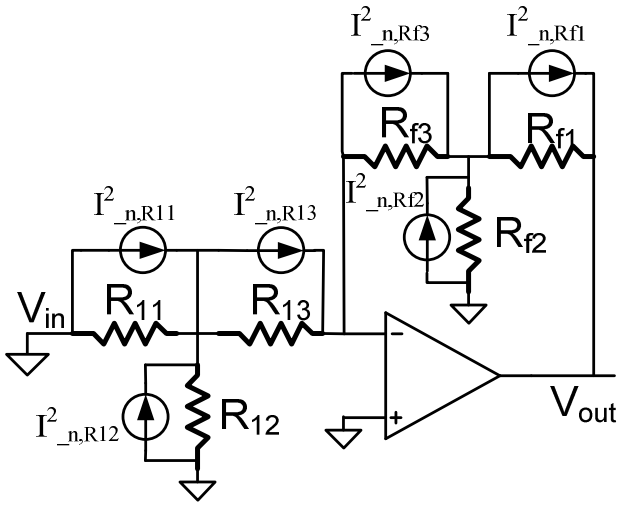

Figure 2- 11 – Noise Model of Resistor Feedback Amplifier Using T-networks.

In Figure 2-11, the transconductance is achieved when (2-32)-(2-33) are hold:

$$R_1 = \frac{R_{11}\cdot R_{13}}{R_{12}} + R_{11} + R_{13}, \qquad (2\text{- }32)$$

$$R_f = \frac{R_{f1} \cdot R_{f3}}{R_{f2}} + R_{f1} + R_{f3}. \quad (2\text{- }33)$$

The noise analysis will start from the input transconductance network, in which R_{11} and R_{12} can be considered as parallel connected because both are connected to ground. And this paralleled resistor will serious connected with R_{13}. The parallel connected total noise current and equivalent resistors are given as (2-32) and (2-33):

$$I_{n11}^2 + I_{n12}^2 = 4KT\left(\frac{1}{R_{11}} + \frac{1}{R_{12}}\right), \quad (2\text{- }34)$$

$$R_{11} // R_{12} = \frac{R_{11} \cdot R_{12}}{R_{11} + R_{12}}. \quad (2\text{- }35)$$

Then the two noise current sources will pass the equivalent resistor given by (2-33) and it is series connected with R_{13} then. Thus it is more convenient to express this noise source in voltage so that it can be added directly with the noise source from R_{13}. The input T-network and the total equivalent noise sources can now presented as below:

$$V_{n1,tot}^2 = V_{n11//12}^2 + V_{n13}^2 = 4KT\left(\frac{R_{11} \cdot R_{12}}{R_{11} + R_{12}} + R_{13}\right), \quad (2\text{- }36)$$

$$R_{eq} = \left(\frac{R_{11} \cdot R_{12}}{R_{11} + R_{12}} + R_{13}\right). \quad (2\text{- }37)$$

For the feedback T-network, the T-Δ transform has been performed here again.

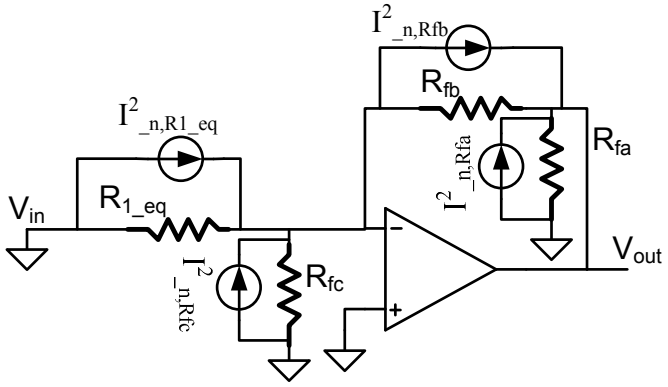

Figure 2- 12-- Noise Model of Simple Resistor Feedback Amplifier with Single Stage T-networks.

The values of R_{fa}, R_{fb} and R_{fc} are listed below:

$$R_{fa} = \frac{R_{f1}\cdot R_{f2} + R_{f2}\cdot R_{f3} + R_{f3}\cdot R_{f1}}{R_{f1}} = \left(R_{f2} + R_{f3} + \frac{R_{f2}R_{f3}}{R_{f1}} \right), \quad (2\text{- }38)$$

$$R_{fb} = \frac{R_{f1}\cdot R_{f2} + R_{f2}\cdot R_{f3} + R_{f3}\cdot R_{f1}}{R_{f2}} = \left(R_{f1} + R_{f3} + \frac{R_{f1}R_{f3}}{R_{f2}} \right), \quad (2\text{- }39)$$

$$R_{fc} = \frac{R_{f1}\cdot R_{f2} + R_{f2}\cdot R_{f3} + R_{f3}\cdot R_{f1}}{R_{f3}} = \left(R_{f1} + R_{f2} + \frac{R_{f1}R_{f2}}{R_{f3}} \right). \quad (2\text{- }40)$$

Three noise current sources, $I^2_{n,R1eq}$, I^2_{nfa}, I^2_{nfb}, will flow through the R_{fb} and contribute to total output noise and the total output noise is derived as:

$$\begin{aligned} V^2_{n,tot} &= \left(I^2_{nR1eq} + I^2_{nfa} + I^2_{nfb} \right)\cdot R^2_{fb} \\ &= 4KT \left[\frac{\left[\frac{\left[R_{f1}R_{f2} + R_{f1}R_{f3} + R_{f2}R_{f3} \right]}{R_{f2}} \right]^2}{\frac{R_{11}R_{12}}{R_{11}+R_{12}} + R_{13}} + \frac{[R_{f1}R_{f2} + R_{f1}R_{f3} + R_{f3}R_{f2}]R_{f1}}{R^2_{f2}} + R_{fb} \right]. \end{aligned} \quad (2\text{- }41)$$

Beware of the factor that R_{fb} equals to R_f, the noise level in Figure 2-11 and Figure 2-10 will be determined by comparing the first two components in the bracket of (2-41) with the term "R^2_f/R_1" in (2-31). In order to simplify the analysis, assume that $R_{11}=R_{13}=aR_{12}$, and

$R_{f1}=R_{f3}=aR_{f2}$, with combing (2-32) and (2-33), the term "R^2_f/R_1" then can derive as following:

$$\frac{R_f^2}{R_1}=\frac{\left[\frac{[R_{f1}R_{f2}+R_{f1}R_{f3}+R_{f2}R_{f3}]}{R_{f2}}\right]^2}{\frac{R_{11}R_{13}+R_{11}R_{12}+R_{12}R_{23}}{R_{12}}}=(a^2+2a)\frac{R_{f2}^2}{R_{12}}. \qquad (2\text{-}42)$$

And the first two terms in the bracket of (2-41) can be simplified as following:

$$\begin{aligned}&\frac{\left[\frac{[R_{f1}R_{f2}+R_{f1}R_{f3}+R_{f2}R_{f3}]}{R_{f2}}\right]^2}{\frac{R_{11}R_{12}}{R_{11}+R_{12}}+R_{13}}+\frac{[R_{f1}R_{f2}+R_{f1}R_{f3}+R_{f3}R_{f2}]R_{f1}}{R_{f2}^2}\\ &=\frac{\left[\frac{aR_{f2}^2+a^2R_{f2}^2+aR_{f2}^2}{R_{f2}}\right]^2}{\frac{aR_{12}^2+a^2R_{12}^2+aR_{12}^2}{(a+1)R_{12}}}+\frac{(a^2+2a)R_{f2}^2\cdot aR_{f2}}{R_{f2}^2} \qquad (2\text{-}43)\\ &=(a^2+2a)(a+1)\frac{R_{f2}^2}{R_{12}}+(a^2+2a)aR_{f2}\end{aligned}$$

For unit gain resistor feedback amplifier, we have $R_{f2}=R_{12}$, and then total output noises of single resistor and T-network are given in (2-44) and (2-45), respectively.

$$V_{o,n,tot\_single}^2=4KT\left[(a^2+2a)R_{f2}+R_f\right]=4KT\left[2(a^2+2a)R_{f2}\right], \qquad (2\text{-}44)$$

$$V_{o,n,totT}^2=4KT\left[(a^2+2a)\cdot(2a+1)R_{f2}+R_{fb}\right]=4KT\left[2(a+1)(a^2+2a)R_{f2}\right]. \qquad (2\text{-}45)$$

Comparing (2-44) with (2-45), it is clearly shown that the total noise of the circuit using T-networks has increased the total thermal noise associated with the passive components by a factor of *(a+1)*.

Beside the passive components, another major noise contributor is the op amp. The relationship between the transconductance networks and the noise due to the opamp will be exploited in the following.

For the simplicity, the noise sources of the amplifier will be presented as a single voltage noise source at the positive input port as shown below:

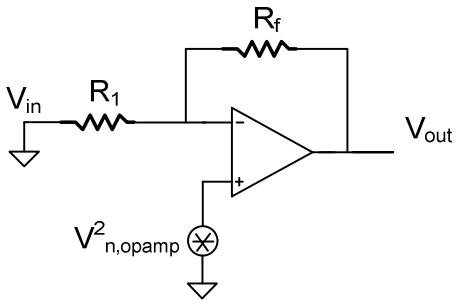

Figure 2- 13 -- Noise Model of Simple Resistor Feedback Amplifier with Noisy Opamp

In Figure 2-13, single resistors are used and the total output noise due to the opamp is given by:

$$V_{OUT,n}^2 = V_{n,amp}^2 \left(\frac{R_f + R_1}{R_1} \right)^2 . \qquad (2\text{- }46)$$

After the T-networks have replaced those single resistors and the same transform process has been done, the equivalent noise circuit is shown below:

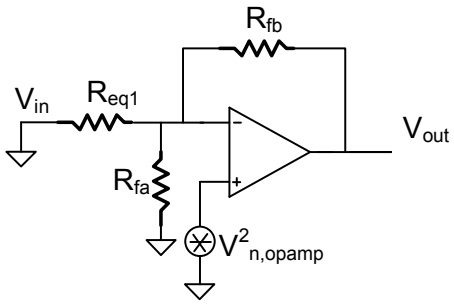

Figure 2- 14 -- Noise Model of Simple Resistor Feedback Amplifier After Y-Δ Transformation.

The total output noise due to the opamp is then given:

$$V^2_{OUT,n} = \left(1 + \frac{R_{fb}}{R_{fa}} + \frac{R_{fb}}{R_{eq1}}\right)^2 \cdot V^2_{n,amp}. \quad (2\text{-}47)$$

With the summation of (48) and (33), the total noise of unit gain resistor amplifier is given:

$$V^2_{out,tot,\sin gle} = 4KT(2R_f) + V^2_{n,amp}4. \quad (2\text{-}48)$$

Also the total output noise with the symmetrical T-networks resistor amplifier is shown below from (2-45) and (2-47):

$$V^2_{out,tot,n} = 4KT(2R_f)(a+1) + V^2{}_{n,amp} \cdot 4(a+1)^2. \quad (2\text{-}49)$$

Through the comparison of (2-48) and (2-49), we can see that the noise associated with the passive components and opamp has been increased be the factor of *(a+1)* and *$(a+1)^2$* respectively. Similar with the trade off between the linearity and area efficiency discussed in the previous section, the trade off also exist between the noise performance and area since the higher value of *a*, the more area will be saved with the transconductance networks. This magnify effects on the noise level will be verified through the following experiment. A simple resistor feedback circuit with both single resistors and transconductance networks as shown in Figure 2-3 (a) has been built using discrete components. The opamp is chosen AD8032A from Analog Device Inc. and the spectrum analyzer, HP 3585A has been used to test the noise spectrum density. The noise from the signal generator; HP33120A, and internal noise of the spectrum analyzer are added to (2-49):

$$V^2_{out,tot,n} = 4KT(2R_f)(a+1) + V^2{}_{n,amp} \cdot 4(a+1)^2 + V^2_{n,source} + V^2_{n,\text{int}ernal}. \quad (2\text{-}50)$$

The input and feedback resistors are chosen as 1 MΩ and the input voltage noise of the opamp is 15 nV/√Hz. There are total 5 different single-stage T-network have been tested with the value of *a* ranging from 8 to 100. The theoretical values resulted from (2-50) and the measured results are shown in Figure 2-15.

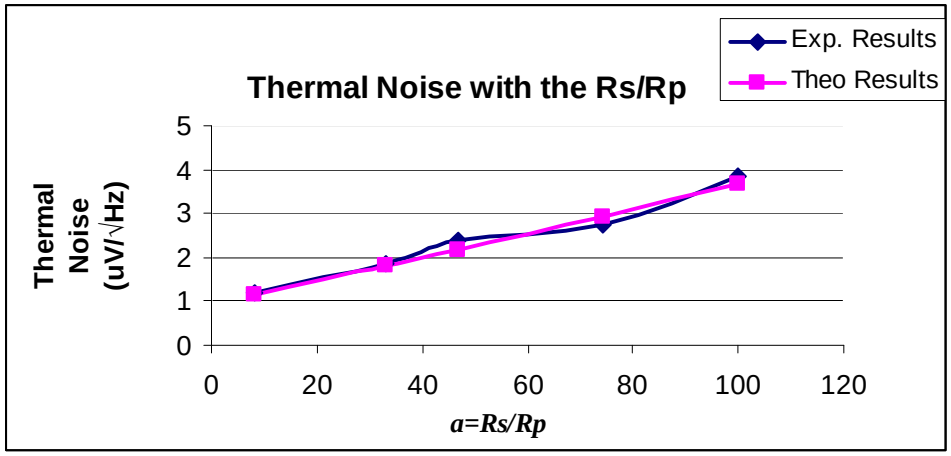

Figure 2- 15 -- Noise Spectrum Density Vs a of Single-stage T-network.

From Figure 2-15, the measurements match the theoretical results very well and it is clearly shown that the trade off between the noise and area efficiency with transconductance networks.

For above experimental results, the noise from the amplifier is comparably small compared to the noise from passive components. It is more efficient to use low noise amplifier with the transconductance networks if the noise is of major concern since the noise from the amplifier will be increased by a factor of $(1+a)^2$ and that will be dominant with even moderate large value of *a*.

The noise problem will be further studied by assuming that the major noise contributing to the amplifier are from the input pair and the current source pair. It is well known that by increasing geometrical ratio of the input differential pair transistors, the input

referred noise will reduce. Therefore, there is a trade off between the area used for passive transconductance networks and the active input transistors if the total output noise is fixed. A simple fully differential input, single end output amplified is shown below with major noise sources.

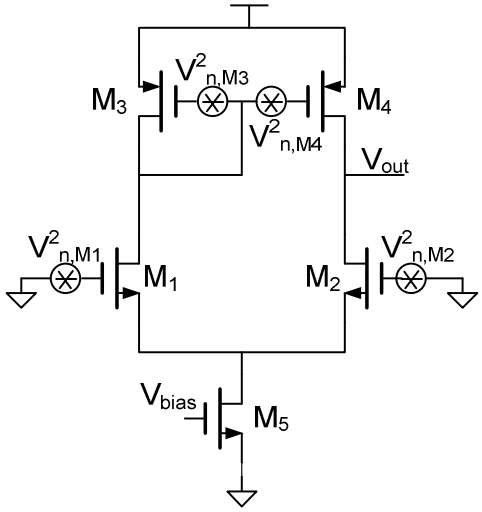

Figure 2- 16 -- Noise Sources of Simple Amplifier.

The gain of noise source at current source pair $M_{3,4}$ to the output is given by:

$$A_{n,M3,4} = \frac{g_{m3,4}}{g_o}. \tag{2- 51}$$

Here, go represents the equivalent output conductance comprised mostly by M_2 and M_4. Assume M_3 and M_4 are perfectly matched and the total output thermal noise is presented in (2-52):

$$V_{n,out,opamp}^2 = 4KT\left(\frac{2}{3g_{m1}} + \frac{2g_{m3}}{3g_{m1}^2}\right). \tag{2- 52}$$

Now the issue about the increase of the active area to compensate the noise enhanced due to the transconductance networks is discussed. In order to relate the noise of the opamp to the area, all the g_m will be expressed as:

$$g_m = \sqrt{\left(\frac{W}{L}\right) 2\mu C_{OX} I_D} \,. \tag{2- 53}$$

And the now the total output thermal noise is expressed as:

$$V_{n,out}^2 = 8KT\left(\Big/ \frac{1}{\sqrt{\left(\frac{W}{L}\right)_1 2\mu_n C_{OX} I_{D_1}}} + \sqrt{\left(\frac{W}{L}\right)_3 2\mu_p C_{OX} I_{D3}} \Big/ \left(\frac{W}{L}\right)_1 2\mu_n C_{OX} I_{D1} \right). \tag{2- 54}$$

Assume $(W/L)_3/(W/L)_1=\theta$, $\mu_n/\mu_p=k$, and $I_{D1}=I_{D3}$. If the total output thermal noise if fixed, so the input transistors W/L ratio has be to increased by a factor of α to compensate the enhanced noise due to the transconductance with a series to parallel ratio a. The equation can be derived as:

$$\frac{1}{\sqrt{\alpha}} + \frac{\sqrt{\theta \cdot k}}{\alpha} = \frac{1+\sqrt{\theta \cdot k}}{(a+1)^2} \,. \tag{2- 55}$$

The value of α can be solved from (2-55) for certain process and design in which case, the value of θ and k is determined. Thus the designer can use this value to estimate the area needs to allocate with active components, especially input pair, for certain and compare it with the area saving by the transconductance networks and by judging those two, the optimum area can be achieved with the noise constrains.

Circuits shown in Figure (2-10) and (2-11) are simulated using Cadence to verify the analysis in above by using the amplifier shown in Figure 2-16. The single resistor was set to 1 M Ohm in order to test the noise performance when this technique is used in audio frequency range. For T-network, $R_{11}=R_{13}=R_{f1}=R_{f3}=10K$, $R_{12}=R_{f2}=100$, thus a is set as 10K/100=100. The amplifier is telescope cascade two stage amplifier as shown in figure V-3-

7. For single resistor, the total noise calculated from (2-46) for ideal op amp and integrated to 5 KHz should be 13 uV.

From (2-49), we will predict the total noise of the T-network will be √(a+1) times greater than what for the single resistor. In this example, a=100, so the total output noise voltage integrated up to 5 KHz is about 130 uV. For more accurate analysis, the *1/f* noise should be included also from the input pair of the amplifier:

$$V^2_{n,1/f} = \frac{K}{WLC_{ox} f} \cdot \tag{2- 56}$$

Then the same as thermal noise, this noise will be amplified by $(a+1)$ times. After all the coefficients have been set as: $K=1.38*10^{-23}$, W=4*31.8 um, L=1.2 um, $C_{ox}=3.9\varepsilon_0/T_{ox}= 2.4665\times10^{-3}\ pF/um^2$, the calculation results and simulation results are listed to do the comparison in the Table 2-2. (g_{m1}=2.412m, g_{m3}=1.33m).

Table 2- 2 Calculated Noise Compared with Simulated Noise.

Noise Analysis and Simulation Results				
Resistors	**Ideal Opm**		**Real opm (GB=95M)**	
Total output noise	Calculation (uV)	simulation (uV)	Calculation (uV)	Simulation (uV)
Single R (R=1 M)	13	12.96	20	20.23
T-network (Rp=100, a=100)	130	130	1555	1575
T-network (Rp=1000, a=30)	84.9	73	479	478
T-network (Rp=12500, a=8)	39	38.8	144	145.3

Table 2-2 shows the highly agreements between the calculated outputs and the simulated results. In the previous sections, the linearity and noise trade off with area has been addressed and we can see the more area saved, the higher distortion and noise level would be expected.

From above discussion, we know that high area efficiency will be obtained with the price of linearity and noise performance. However, there is still another trade off interested and worth being paid attention, the trade off between the linearity and noise. In the previous sections, the symmetrical T-networks, in which case, two series resistors have the same value, are chosen for the simplicity. Those two series resistors are not necessary to be the same in real design and if asymmetrical T-networks are chosen, there is one more design freedom than the symmetrical transconductance networks. Again, the transconductance networks replace the single resistors as shown in Figure 2-3 (a), and the ratios of series resistor over shunt resistor are $R_{11}=aR_{12}$, $R_{13}=bR_{12}$. After Y-Δ transformation, the relationships of the resistors in Figure 3 (b) are given below, if assume $R_{12}=R_{22}=R$ and for unit gain feedback:

$$R_a = R + bR + \frac{b}{a}R, \tag{2- 57}$$

$$R_b = aR + bR + abR, \tag{2- 58}$$

$$R_c = R + aR + \frac{a}{b}R. \tag{2- 59}$$

The same analysis is presented and the new value of shunt resistors in Figure 4 is derived:

$$R_{shunt} = R_{1c} // R_{2c} = \frac{1}{2}\left(a + 1 + \frac{a}{b}\right)R. \tag{2- 60}$$

The equivalent feedback factor β_T is calculated:

$$\beta_T = \frac{R_{1b}R_{shunt}}{R_{1b}R_{shunt} + R_{2b}R_{shunt} + R_{1b}R_{2b}}$$

$$= \frac{1}{2}\frac{ab+a+b}{a+b+ab^2+2ab+b^2}. \quad (2\text{- }61)$$

The term "$ab+a+b$" is actually the resistor scaling factor θ defined in (2-2) and (2-60) can be modified as:

$$\beta_T = \frac{1}{2}\frac{\theta}{\theta + b\cdot\theta} = \frac{1}{2}\cdot\frac{1}{1+b}. \quad (2\text{- }62)$$

It is interesting that the feedback β_T is proportional to the reverse of b and independent of another T-network parameter a. If the linearity is the first priority among the specifications and the area efficient is limited somehow by linearity, noise and amplifier characteristics, the larger the R_{11} should be chosen to result the larger β_T and the better linearity. In the next part, the noise performance will be analyzed with asymmetrical T-networks.

Rewrite (2-41), however, the equivalent resistor in Figure 2-12 are different as those in the previous sections as shown below:

$$R_{11} = aR_{12}, R_{13} = bR_{12}, R_{f1} = aR_{f2,}\ R_{f3} = bR_{f2}, \quad (2\text{- }63)$$

$$R_{fa} = \left(1+b+\frac{b}{a}\right)R_{f2}, \quad (2\text{- }64)$$

$$R_{fb} = (a+b+ab)R_{f2}, \quad (2\text{- }65)$$

$$R_{fc} = \left(1+a+\frac{a}{b}\right)R_{f2}. \quad (2\text{- }66)$$

The total output thermal noise due to the passive components then is given by (2-67):

$$V_{n,out,R}^2 = 8KT(a+b+ab)(a+1)R_{f2}$$

$$= 8KT[\theta(a+1)]R_{f2}. \quad (2\text{- }67)$$

Using the same approach with the noise due to the amplifier, the noise due to the amplifier is then given:

$$V_{n,out,opamp}^2 = 4 \cdot V_{n,opamp}^2 (a+1)^2 . \quad (2\text{- }68)$$

The total output noise is the summation of (2-67) and (2-68) and expressed in (2-69):

$$V_{n,out,tot}^2 = 8KT[\theta(a+1)]R_{f2} + 4 \cdot V_{n,opamp}^2 (a+1)^2 . \quad (2\text{- }69)$$

It is clearly shown that the total output noise is only proportional with the T-network coefficient *a* and independent of another coefficient *b*. Therefore, with the fixed area efficiency, a better noise performance will be achieved with the larger resistor R_{13} in Figure 2-3. Combining both (2-62) and (2-69), the trade off between the linearity and noise is brought forward. For a given area efficiency, the linearity can be boosted further by put a larger resistor of R_{11} in Figure 2-3 and a smaller resistor of R_{13} to maintain a certain equivalent transconductance. While for the concern of noise performance, the larger resistor should be put behind the shunt resistor in the T-network. An experimental result exhibiting this linearity-noise trade off will be shown in the following part. The total equivalent transconductance is set to be 1 u and the same opamp and spectrum analyzer has been used in this test. There are two sets of different T-networks are included. For the first set, three resistors values are: R_{11}*=10 KΩ,* R_{12}*=1 KΩ,* R_{13}*=90 KΩ* and the second set resistors values are: R_{11}*=22 KΩ,* R_{12}*=1 KΩ,* R_{13}*=47 KΩ*. The simplest method to testify this trade off is just to sweep the R_{11} and R_{13} and measure the noise and harmonic distortions in each resistor set up. The noise and linearity will be plot out with the change of the ratio of R_{11}/R_{12}, a, and this trade off relationship is shown in Figure 2-17 below.

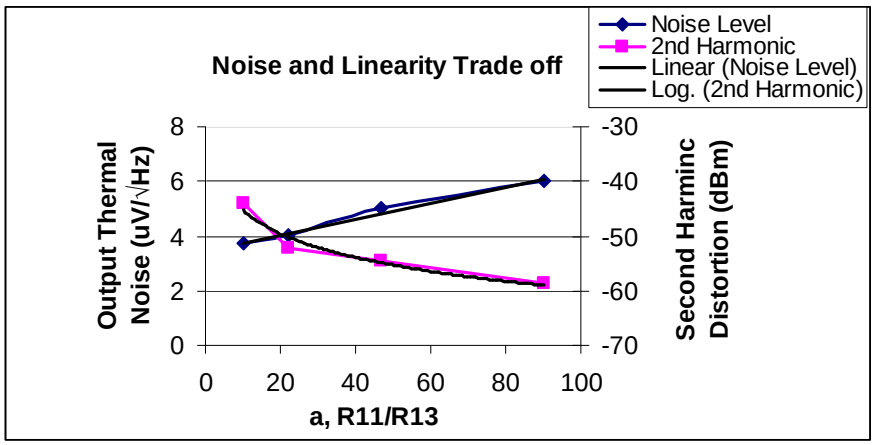

Figure 2- 17 -- Noise and Linearity Trade-off with Asymmetrical T-networks.

From Figure 2-17, after the fit-line was used, the noise increased approximately linear with the value of *a* and the second harmonic distortion decreased roughly in log relationship with *a*. Those match the analysis for linearity and noise given in (2-29) and (2-50) and demonstrate a design freedom to choose high linearity or low noise according to different applications even with the area efficiency constrained.

2.5 Mapping Between the Design Space and Performance Spaces

In the previous section, the relationships between the linearity and noise and transconductance networks have been discussed. From both the analytical and experimental results, different trade offs are exhibited among the linearity, noise and area efficiency. Trade off is the basic design strategy for circuit designers and there are all kinds of trade off in the circuit design works. The most fundamental trade off is between the design space, which contains all kinds of design parameters, and the performance spaces, which encloses all the specifications. It is very interesting to exploit the mapping between the design space and performance space. Two possible kinds of mappings are shown in Figure 2-18 below:

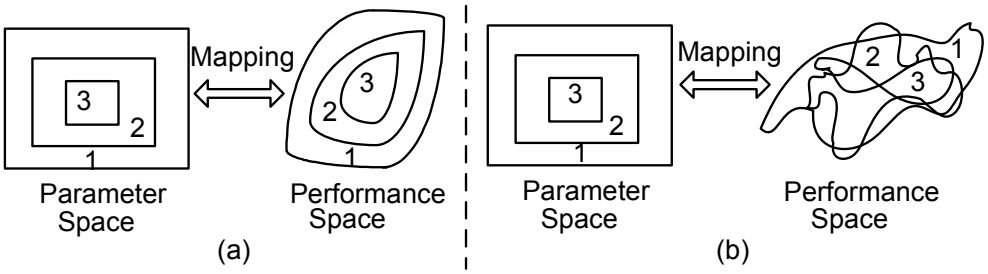

Figure 2- 18 -- Two Kinds of Parameter Space Mapping to Performance Space.

In Figure 2-18(a), a very regular mapping between the parameters space to performance space has been shown. In this kind of mapping, when the design parameters get more stringent values, the performance space also reduce to certain direction and this tendency of the change is monotonic. Or reversely say, when the higher performance is required, the more stringent design parameters are always expected. In the Figure 2-18(b), the mapping between the parameter space and the performance space are irregular. In this case, when the design parameters are getting less flexible, the performance space is not always changing to certain direction. In another word, a regular design parameters space will map to a twisted, non-monotonic performance space. The second situation is certain unfriendly for the circuit designers because it will make the design process with no predictable direction and furthermore every change of performance specification will result lots of redesign. On the contrary, the regular mapping is much easier for the design procedure because the changing of the performance associate with certain design parameters is predictable and the designer can always change the design parameters to certain direction for each re-define specification. Even though, the common experience suggest that almost all the circuit design works are somehow based on the first mapping property, surprisingly no reported work really addressed this issue. In the following part, the mapping characteristics between the parameter space and performance space will be shown. Because the analytical

work in the previous sections have proved that the trade off between certain design parameter and circuit performance can be described as a simple mathematical equations such as (2-29), (2-50) and will not be repeated here, etc, the computer simulations will be used to exploit this mapping properties.

A continuous time low pass active filter has been chosen as the prototype design for the study of the parameter space and performance space mapping, in which the resistor will be implemented either with single resistor or transconductance networks, as shown in Figure 2-19.

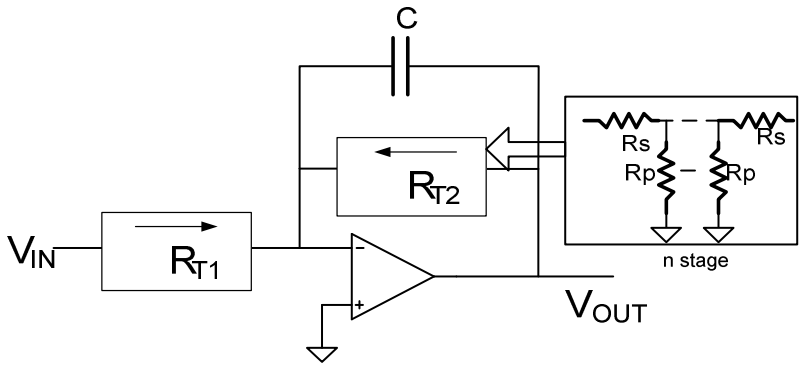

Figure 2- 19 -- Prototype Circuit for Study of Parameter and Performance Space Mapping.

The first step is to define the proper parameter space and performance space for above circuit. The performance space is represented as $P\{p_1, p_2, p_3,\ldots,p_n\}$; $p_1, p_2,\ldots p_i$ represent the performance specifications such as THD, SNR, Area, process variation δ, etc. The parameter space $X\{x_1,x_2,x_3,\ldots,x_n\}$; $x_1, x_2, \ldots,x_n$ contains the design parameters such as number of ladders n, ratio of R_s over R_p, a, unit resistor sheet width w, parallel resistor R_p, etc. Theoretically, the performance specifications are the functions of the design parameters and can be described as following:

$$\delta_{\frac{R_{eq}}{R_{eqN}}} = f_1(R_{REF}, n, a, w), \quad (2\text{-}70)$$

$$SNR = f_2(R_{REF}, n, a, w), \quad (2\text{-}71)$$

$$Area = f_3(R_{REF}, n, a, w), \quad (2\text{-}72)$$

$$THD = f_4(R_{REF}, n, a, w). \quad (2\text{-}73)$$

If function f_1-f_4 can be derived with close form expressions, the mapping between this 4 dimensional parameter space and performance space will be clearly depicted. However, deriving those close form expressions is not very practical and even the close forms are available, it is not straightforward to determine the characteristics. So the simulation will be the first choice to study this problem. For the circuit shown in Figure 2-19, assume the transfer is given, the design parameter space is defined as: $X\{C, R_{T1}, R_{T2}, w, a, n\}$. Some constrains has to be set to set in order to explore the relationship between the performance space and the parameter space. Because the purpose of this paper mainly focuses on the transconductance network, the value of the capacitor will be fixed as 3.5 *pF*. For a given transfer function, the corner frequency and the DC gain are then defined. Therefore, the equivalent transconductance of R_{T1} and R_{T2} are determined. From precious discussion, it is obvious that the shunt resistor (R_p), ratio of series resistor to the shunt resistor (a) and the total number of stages (n) will determine the overall transconductance value. If assume the series resistors are comprised of the unit shunt resistors, the width of the poly to implement the shunt resistor (w) will determine the total passive component area. The parameter space then is defined as: $X\{ w, a, n\}$ and the performance space is given as *P{Area, THD, SNR, process deviation(δ)}*. In order to simplify the problem, different 2 dimensional mapping will be presented in the

following part instead of the multiple dimensional mapping, which is not easy to be described and understood.

The first mapping is focus on the linearity and total transconductance area in the performance space. From the section 2, we know the total T-network area is given:

$$A_T = A_{REF} \cdot \frac{\theta}{\eta}. \tag{2- 74}$$

And A_{REF} denote the area of reference shunt resistor and it is given by:

$$A_{REF} = \frac{R_{REF}}{R_d} \cdot W_{unit}. \tag{2- 75}$$

Here, R_d is the sheet resistance and it is 30 Ω/□ for AMI 0.6 um process and the W_{unit} represents the width of the poly resistor square and it is chosen as 1.2 um for this simulation. The circuit shown in Figure 2-19 has been simulated with the transconductance networks with different value of *a*, *n* and *Rp*. The linearity and total transconductance area are shown in the figures below.

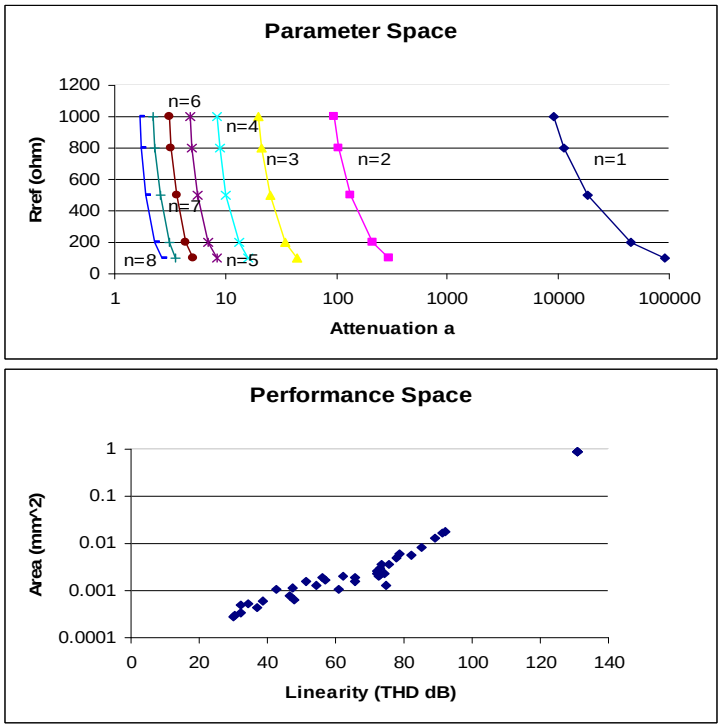

Figure 2- 20 -- {Rp, n, a} Space Mapping to {THD, Area} Space, set I.

Above figure shows the first set mapping in the Parameter Space, the number of stage n ranges from 1 to 8, the reference resistor values changes from 100 to 1000, and the a is dependent variable with *a* given transconductance value. Because *n* is an integer number, the parameter space is not cover all the area instead it cover the discrete lines defined by *n*. The performance space is a narrow strip and the area ranges from 0.00027 mm^2 to 1 mm^2 and the THD ranges from about 30 dB to 140 dB. In the next step, the parameter space will be diminished gradually and the corresponding performance spaces will be shown.

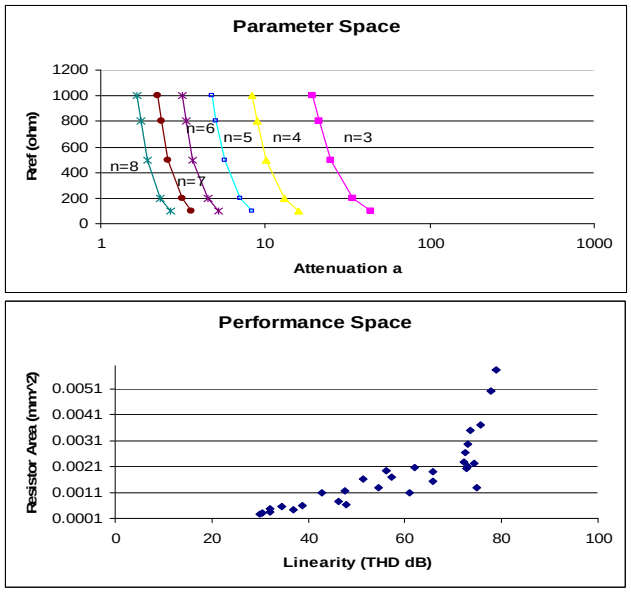

Figure 2- 21-- {Rp, n, a} Space Mapping to {THD, Area} Space, set II.

In this set of mapping, the parameter space is reduced by decreasing the number of stage n, which ranges from 3 to 8 and R_{REF} range remains the same. Correspondingly, the performance space also reduced by losing the most up-right corner and the area ranges from 0.00027 mm^2 to 0.0058 mm^2 and the THD locates between 30 to 79 dB.

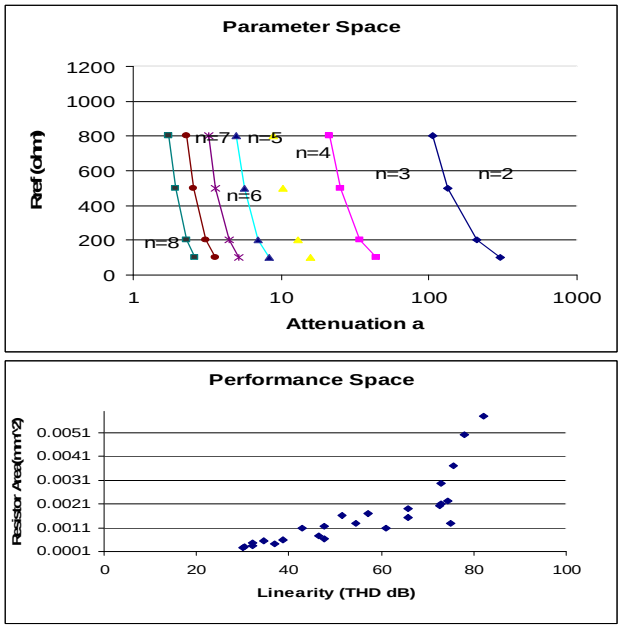

Figure 2- 22 -- {R_p, n, a} Space Mapping to {THD, Area} Space, set III.

In the set III, the parameter space decreases from two different directions: *n* range from 2 to 8 and R_{REF} range from 100 to 800 Ω. The performance space now not only lost the most up right area, but also shrunk to be narrower: THD has a range of [30dB, 91dB], Area has the range of [0.00027mm^2, 0.0163 mm^2]. If the parameter space is further reduced, the mappings between tow spaces are shown below.

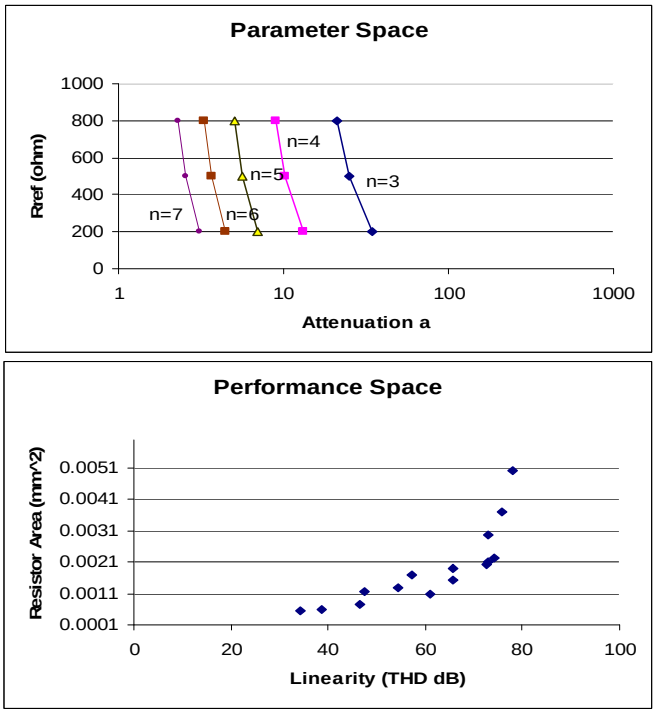

Figure 2- 23 -- {R_p, n, a} Space Mapping to {THD, Area} Space, set IV.

After the design space has been reduced further with *n* range between 3 and 7 and R_{REF} range from 200 to 800, the performance space reduce correspondingly and the THD range from 33 dB to 74 dB and the Area range from 0.0005 mm^2 to 0.005 mm^2.

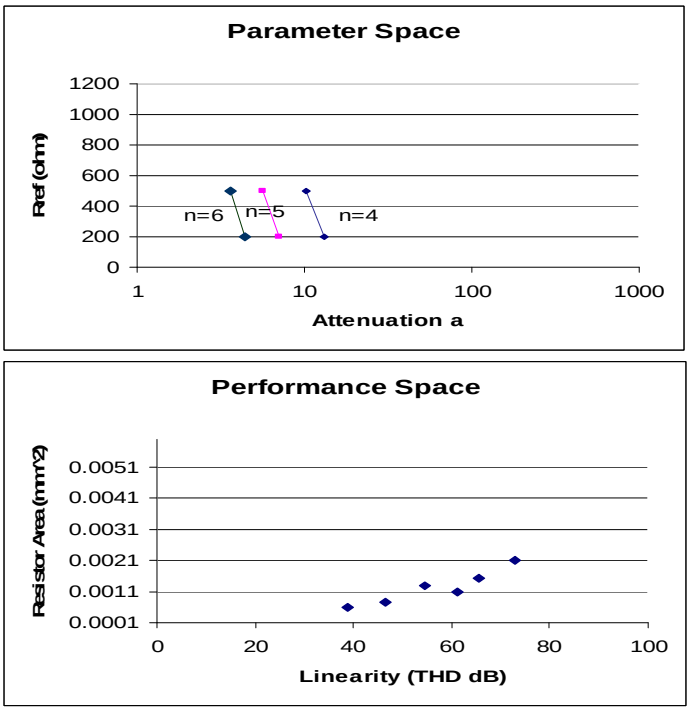

Figure 2- 24 -- {R_p, n, a} Space Mapping to {THD, Area} Space, set V.

With the design parameter space keep shrinking, the performance space also keeps reduce. In Fig. 24, the parameter space contains *n* ranging between 4 and 6 and the R_p locating between 200 to 500 Ω, the corresponding performance space has the THD between 38 to 73 dB and the total transconductance area between 0.00061 mm^2 to 0.0021mm^2. Fig. 20-24 exhibit the mapping between the parameter space {*n*, R_p} to the performance space {*THD, Area*} and it is clearly to show that with the regular reducing the parameter, the performance space will shrink according to each step of the reduction of the parameter space and this diminish is regular and monotonic. The mapping between the space {*n*, R_p} to another performance space {*THD, SNR*} will be presented in the following part.

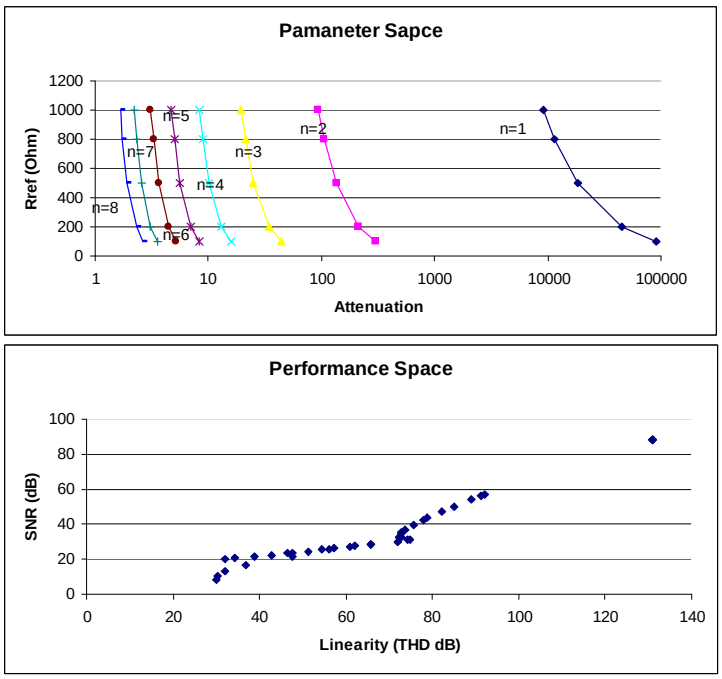

Figure 2- 25 -- {R_p, n, a} Space Mapping to {THD, SBR} Space, set I.

In Figure 2-25, similar with in Figure 2-20, the performance space is a narrow long stripe implying that the number of stage or the R_p value really stretch the performance space {*THD*, *SNR*} just like it did on the performance space {*THD*, *Area*} so that the mapping is expected to be similar. The first step is also to reduce the number of stage as shown below.

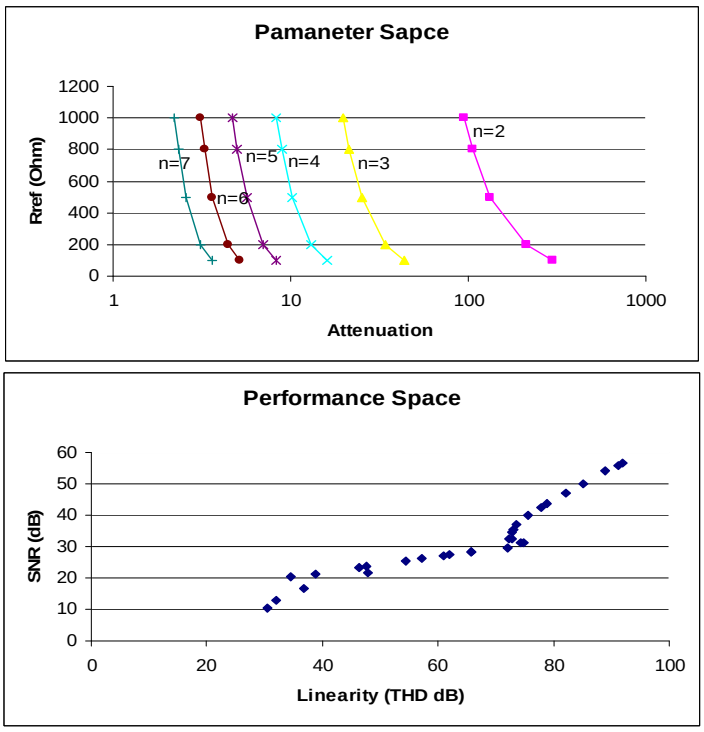

Figure 2- 26 -- {R_p, n, a} Space Mapping to {THD, SBR} Space, set II.

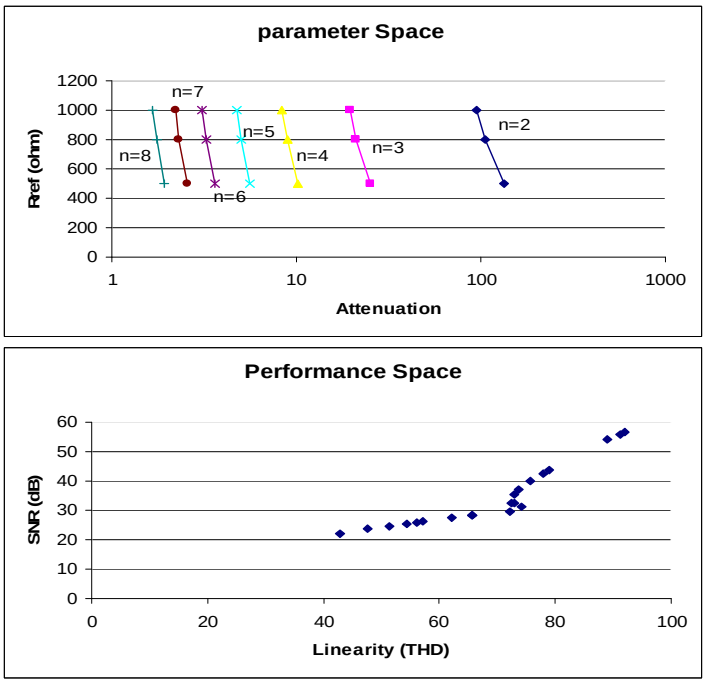

Figure 2- 27 -- {R_p, n, a} Space Mapping to {THD, SBR} Space, set III.

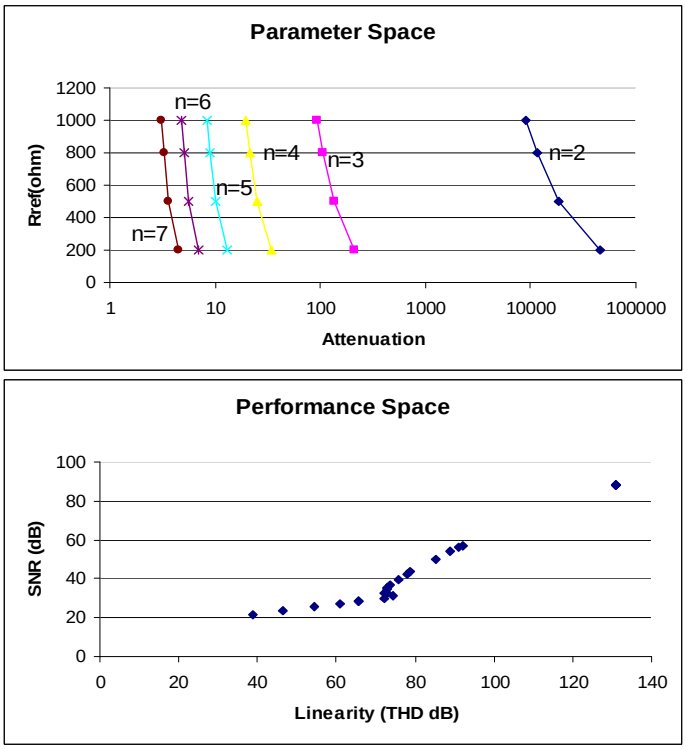

Figure 2- 28 -- {R_p, n, a} Space Mapping to {THD, SBR} Space, set IV.

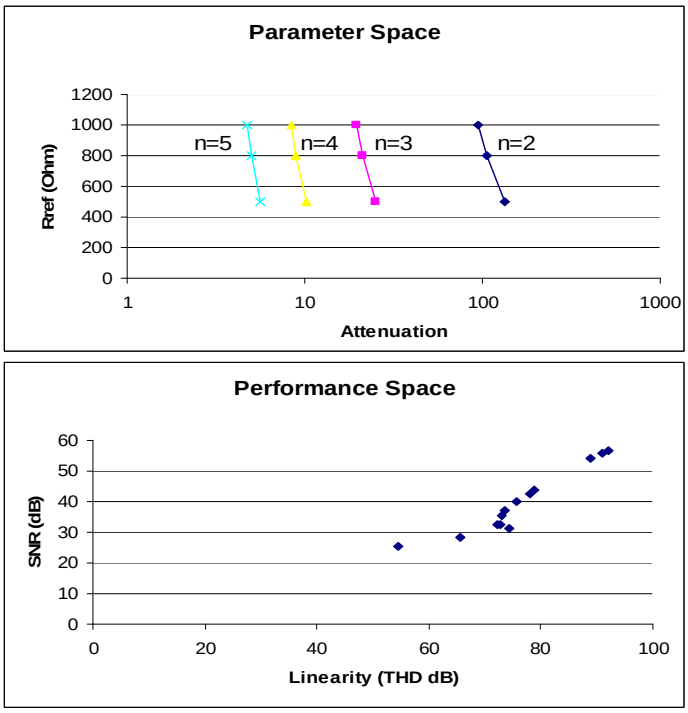

Figure 2- 29 -- {R_p, n, a} Space Mapping to {THD, SBR} Space, set V.

With the reduction of the number of stages, the performance space again shrink from the most up right corner and the linearity range decreases from the original [30dB, 140dB] to [35dB, 94dB] and the SNR also contract from [8dB, 88dB] to [10dB, 60dB]. In the following figures, the parameter space will keep shrinking and the corresponding performance change will be shown. As shown step by step from Figure 2-27 to Figure 2-29, the parameter space reduces from two directions, the number of stages *n* and the shunt resistor value R_{REF}. The performance space will regularly diminishes also in two dimensions, linearity *THD* and the noise performance, *SNR*. The parameter space and performance space in Figure 2-27-Figure 2-29 are tabled below.

Table 2- 3 Parameter Space Mapping to Performance Space

Mapping #	Parameter Space		Performance Space	
	n, # of stage	Rref	THD	SNR
1	[2 , 8]	[100Ω ,1000Ω]	[30dB , 131dB]	[8dB , 88dB]
2	[2 , 7]	[100Ω ,1000Ω]	[30dB , 92dB]	[10dB , 56dB]
3	[2 , 8]	[500Ω ,1000Ω]	[43dB , 92dB]	[22dB , 57dB]
4	[1 , 6]	[200Ω ,1000Ω]	[38dB , 131dB]	[21dB , 88dB]
5	[2 , 5]	[500Ω ,1000Ω]	[54dB , 92dB]	[25dB , 57dB]

With the figures and table above, it is clearly to show that when the parameter space regularly shrinks, the performances space will also diminish regularly according to every step change of the parameter space and this change is monotonic. Back to the prediction in Fig. 18., the mapping for this circuit between the parameter space *{n, R}* and performance space *{THD, Area}* and *{THD, SNR}* is the same as described as *(a)*, even the corresponding performance space is much narrower. Revealing this mapping property will gives the circuit

designers confident to scale the design parameters more efficient when facing the difference specification requirements.

2.6 Transconductance and Process Variation

One of the most popular applications of the transconductance networks are used in the high linear active filters in low frequency applications. Because the transconductance networks will replace the single large value resistors, which are used to define the time constant in the filter, the actual value and the process variations will directly determine the accuracy and the yield of the filters. The are many tuning techniques for adjust the time constant of the active filters due to the process and temperature variations of the poly resistors have been published and they have done good job to overcame this limitation of the poly resistors. To understand the process variations associated with the transconductance networks versus to the single resistors will be very useful in this approach when those existing tuning techniques can be adopted. For example, if the process variation of the transconductance networks is somehow worse than the single resistors, the tuning range will need to be enlarged when it is used to adjust the corner frequency in certain accuracy requirement. In the following part, the process variation of the two most popular transconductance networks will be studied compared to the single resistor.

A major factor that limits the practicality of these networks is their sensitivity to process variations. In this section the sensitivity of these networks to process variations will be considered. Two issues are of particular interest. First is the issue of how the nominal transresistance varies with process. The second is how the transresistance varies with die-level variations.

In regard to the variation with process parameters, it should be noted that the transresistance of all of the ladder-based structures can be expressed as a product of a geometric factor and the resistance of a reference resistor. It thus follows that the process sensitivity of the transresistors is the same as that of a standard resistor in the same process. The issue of die-level variations will now be addressed. The components of die-level variations that is associated with uncorrelated deviations of widely spread devices can be considered as part of random process variations. In what follows we will assume that layout techniques are used in the transresistors to compensate for gradient effects and that the local random variations will be the dominant factor affecting the variability of resistors. It will also be assumed, for convenience, which the edge roughness effects on the resistor boundary are negligible compared to the random variations of the sheet resistance in the resistor body. Under these assumptions, it is well known that the variance of a rectangular resistor of length L and width W and value R_X due to local random variations in the sheet resistance can be expressed as:

$$\sigma^2_{\frac{R_X}{R_{XN}}} = \frac{\mathcal{A}^2_\rho}{A_{R_X}}. \qquad (2\text{-}76)$$

where $\mathcal{A}_\rho$ is a process-dependent constant, R_{XN} is the nominal value of the resistor, and $A_{RX}=WL$ is the area of the resistor. Our goal will thus be to see how the variance of a transresistor compares to that of a basic rectangular resistor. It can be shown that the variance of the transresistance can be expressed in terms of the variance of the reference resistor *R* by the expression:

$$\sigma^2_{\frac{R_{EQ}}{R_{EqN}}} = h\sigma^2_{\frac{R}{R_N}}. \qquad (2\text{-}77)$$

where the term h is dependent upon the architecture of the transresistors but not upon the process. It thus follows from (2-76) and (2-77) that:

$$\sigma^2_{\frac{R_{EQ}}{R_{EQN}}} = h\frac{\mathcal{A}_\rho^2}{A_R}. \tag{2- 78}$$

It can be derived from section 2.2:

$$A_R = \frac{\eta}{\theta}A_{TOT}. \tag{2- 79}$$

Combining (2-77), (2-78) and (2-79), the standard deviation of the equivalent transconductance network can be expressed as (2-80):

$$\sigma^2_{\frac{R_{EQ}}{R_{EQN}}} = \left[\frac{h\theta}{\eta}\right]\frac{\mathcal{A}_\rho^2}{A_{TOT}}. \tag{2- 80}$$

The term in brackets in (2-80) is a variance scaling factor and is dependent only on architecture of the transresistors and the dependence on process and area has the same functional relationship as for a single resistor as evidenced by comparing (2-80) with (2-76). We will now consider the variance scaling factor.

From quite straightforward derivations for $1 \le n \le 3$, the values of h are given in (2-81) and (2-82) for R-2R network and T-structure, respectively, and hand analysis becomes quite tedious for n>3.

$$h_{R-2R} = \begin{cases} 0.5 & n=1 \\ 0.5625 & n=2 \\ 0.707 & n=3 \end{cases}, \tag{2- 81}$$

$$h_T = \begin{cases} \dfrac{1}{a} & n=1 \\ \dfrac{a^3+2(a+1)^2}{a(a+2)^2} & n=2 \\ \dfrac{2a^3+3a^2+4a+2}{a(a+2)^2} & n=3 \\ \dfrac{2a(a^3+5a^2+6a+1)^2+2a(a^3+4a^2+4a+1)^2+2(a^4+4a^3+3a^2)^2+(a^4+4a^3+4a^2)}{(a^4+6a^3+10a^2+4a)^2} & n=4 \end{cases} . \quad (2\text{-}82)$$

Substituting the parameters *h*, θ, and η required in variance scaling factor we obtain from previous analysis and the term in the bracket of (81) can then be expressed as:

$$\left[\frac{h\theta}{\eta}\right]_{R2R} = \begin{cases} 3.45 & n=1 \\ 5.625 & n=2 \\ 9.123 & n=3 \end{cases} . \quad (2\text{-}83)$$

The variance scaling factor is tabulated in Table 2-3 for both the R-2R network and T-structure. The variance scaling factor increases with n and, in the T-structure, also increases with a. In both cases it becomes considerably larger than 1 for large n. This information should be useful for determining the area that must be allocated to the transresistance networks for achieving a predetermined acceptable standard deviation.

Although we will not go into details, it can be shown from (2-78), (2-82) and (2-83) that the variance of R_{EQ} is comparable to that of the reference resistor by observing the values of h are in the vicinity of 1 for both transresistance networks. This suggests the transresistance networks configured discussed in this paper will not provide good matching performance unless a larger area is allocated to the reference resistor and increasing the area allocated to the reference resistor defeats the purpose of the area scaling efficiency. Thus, if digital programming is not used, aggressive area efficiency scaling will be useful only if

there are rather lax tolerances on matching. If digital programming, which is inherent in the ladder transresistance structure, is used, the substantial area benefits of the transresistance networks can be derived.

Table 2- 4 Variance Scaling Factor of Ladder Transconductance Networks.

Variance Scaling Factor				
n	R2R	T (a=)		
		4	10	25
1	3.45	1	1	1
2	5.625	6.7	17.8	47
3	9.123	18.8	52	140

2.7 Conclusion

A transconductance network technique has been introduced to the analog circuit design in the paper and it can significantly reduce the passive components area in the modern CMOS integrated circuit design. With this approach, the high linear area efficient poly resistors can be used with the advantage of its low voltage dependence. The transconductance network will also be influential to other circuit characteristics. This paper presented the analysis of the relationship between the transconductance networks coefficients, such as the number of stages, ratio of series resistor over parallel resistors, etc, and the some most important circuit specifications including the area efficiency, linearity, noise performance, process variations. The close form derived from above analysis shows a very clearly trade off between the area saving property of transconductance networks and the linearity, noise and the process variation. The discrete time circuit has been tested for approving the conclusion about such trade offs and the experimental results match the theoretical prediction very well. Understanding the trade off between the transconductance networks and all other circuit

performance requirements is very helpful for using this technique in the practice circuit design to achieve the satisfied performance with as efficient area as possible.

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CHAPTER 3 AREA OPTIMIZATION FOR ACTIVE FILTERS

3.1 Introduction

As part of a typical interface between the analog world and the digital world, continuous-time filters are widely used for anti-aliasing and reconstruction. Considerable demand exists for more general integrated filters as well. The most popular technique for building audio frequency continuous-time filters is to use either a g_m-C or a MOSFET-C approach. There are two main limitations of these types of filters. The first limitation is the process and temperature dependence of both the transconductance elements and the capacitors. This limitation is often overcome by electronically tuning or adapting either the transconductance elements or the capacitors and several techniques that give reasonable performance have been reported in the literature [1]. The other limitation, poor linearity, has been a problem for many years and although some linearization schemes have been proposed, nonlinearity remains a serious limitation of these two types of filters. These limitations were the major reasons that the switched-capacitor technique has evolved. Specifically, the switched capacitor circuits are known to have very precisely controlled pole and zero frequencies and good linearity. Switched capacitor filters are not without limitations. Switched capacitor filters inherently provide switching noise, require accurate clock generation, and are inherently discrete time rather than continuous-time in nature thus presenting aliasing of high-frequency noise into the frequency band of interest. In some semiconductor processes, good capacitors and/or good switches may not be available as well. The conventional active RC filters are inherently linear and operate in the continuous-time domain and both of these properties are particularly attractive for a host of applications [2].

There are, however, two problems with audio frequency monolithic active RC filters. The first problem is the control of the RC products. In some anti-aliasing applications this may not be of concern and the tuning techniques that are used to tune gm-C and MOSFET-C filters can be readily adapted to tune active RC filters. The second problem is the area required to implement the passive components. Specifically, the large RC time constants needed to operate at audio frequencies range invariably require large valued resistors or large valued capacitors or both. A new strategy has been recently introduced to substantially reduce the total resistance or capacitance values needed to realize a given RC product [3]. Then, the issue of minimizing the area required to realize the passive elements becomes increasingly important if these filters are to become practical in the audio frequency applications.

In the previous two chapters, the detail of implementation of the new strategy recently introduced to substantially reduce the total resistance or capacitance values needed to realize a given RC product [3] and the trade off between the design of the transconductance networks and other circuit design parameters have been discussed. Then, the issue of minimizing the area required to realize the passive elements becomes increasingly important if these filters are to become practical in the audio frequency applications.

Closed-form solutions have shown that for some simple first-order filter structures, the active area will be minimized if the resistor area equals the capacitor area. Conventional wisdom also suggests that this may be true in a more general case as well but there does not appear to be any formal mathematical prove to support this wisdom in literature and often this wisdom has been gathered from computer simulations for specific filter structures. In the previous works, there were no considerations for optimizing the total area for passive

elements in literatures even when area is not an ignorable issue, whether for high frequency range RC filters [4] or lower frequency applications [5]. In the following section, the optimal area allocation for several different first-order and second-order active filters is investigated including the first order active filter with or without transconductance networks, and the several popular second order active filters. With this approach, the total passive components area can be further reduced based on the technique introduced in the Chapter 1 and Chapter 2 so that the polysilicon resistor can be widely used in the standard CMOS process even in the very low frequency applications and the circuits could benefit from the high linearity of this passive components with manageable area.

3.2 Optimum Passive Area of the First Order Structures

3.2.1 Single Pole Circuit

In this section, the single pole system will be discussed and the mathematic close form solutions are presented.

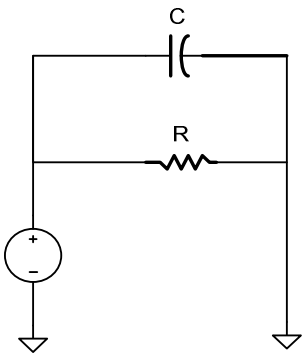

Figure 3- 1 -- First Order Passive Network

The total passive area is the summation of the area of the resistor R and the capacitor C. If the resistance density and capacitance density are R_d and C_d respectively, the total area $A_T=A_R+A_C$, given by the expression:

$$A_T = \frac{R}{R_d} + \frac{C}{C_d}. \tag{3- 1}$$

Since the pole is determined by the RC product, we introduce the constraint RC=K where K is a predetermined value. The optimum area allocation is obtained by taking the partial derivatives of A_T with respect to R and C and then setting these equal to zero subject to the constraint mentioned. We obtain the well-known result for minimizing the total active area A_R=A_C. This equal area allocation is independent of the value for K, R_d and C_d.

3.2.2 Single Pole Active Filter

We will next consider the first-order active filter comprising two resistors and one capacitor shown in Figure 3-2.

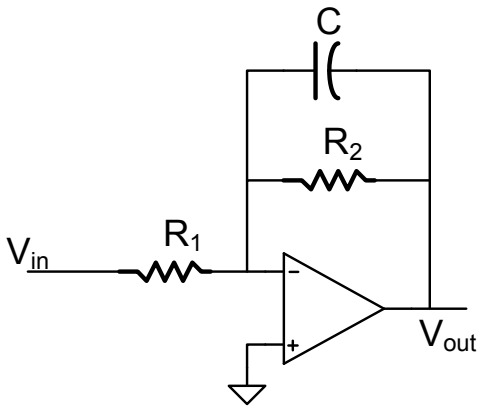

Figure 3- 2 -- First Order Active Filter.

The transfer function of this filter is given by the expression

$$\frac{V_o}{V_i} = -\frac{\frac{1}{R_1 C}}{s + \frac{1}{R_2 C}}. \tag{3- 2}$$

For this transfer function, there are three design variables, R_1, R_2, and C. If the bandwidth and DC gain are set, we will have two constrains:

$$\frac{R_2}{R_1} = K_1 \quad . \tag{3- 3}$$

$$R_2 C = K_2 \ . \tag{3- 4}$$

where, K_1 and K_2 are constants. It follows that the total area for the RC constants is given by the expression

$$A_T = A_R + A_c = \frac{R_1 + R_2}{R_d} + \frac{C}{C_d} \ . \tag{3- 5}$$

where, A_T is the total area, A_R is the total area for the resistors and A_C is the total area for capacitors. Similarly, R_d and C_d are resistor density and capacitance density, respectively. Using Lagrangian multipliers, to embed the constraints, we build the Hamiltonian function as shown below:

$$H = A_T + \lambda_1 (\frac{R_2}{R_1} - K_1) + \lambda_2 (R_2 C - K_2) \ . \tag{3- 6}$$

Taking the partial derivatives with respect to R_1 and R_2 we obtain the expressions

$$\frac{\partial H}{\partial R_1} = \frac{1}{R_d} + \lambda_1 (-\frac{R_2}{R_1^2}) \ . \tag{3- 7}$$

$$\frac{\partial H}{\partial R_2} = \frac{1}{R_d} + \lambda_1 (\frac{1}{R_1}) + \lambda_2 C \ . \tag{3- 8}$$

Setting these two derivatives to zero we obtain

$$\frac{R_1}{R_d} = \frac{\lambda_1 R_2}{R_1} = \lambda_1 K_1 , \tag{3- 9}$$

$$\frac{R_2}{R_d} = \frac{-\lambda_1 R_2}{R_1} - \lambda_2 C R_2 = -\lambda_1 K_1 - \lambda_2 K_2 \ . \tag{3- 10}$$

It thus follows that the total resistor area is given by

$$A_R = A_{R_1} + A_{R_2} = \frac{R_1 + R_2}{R_d} = \lambda_1 K_1 - \lambda_1 K_1 - \lambda_2 K_2 = -\lambda_2 K_2 . \qquad (3\text{-}11)$$

The same operations can be applied to the capacitor resulting in (3-12)

$$\frac{\partial H}{\partial C} = \frac{1}{Cd} + \lambda_2 R_2 = 0 . \qquad (3\text{-}12)$$

Thus, we obtain the total capacitor area:

$$A_C = \frac{C}{C_d} = -\lambda_2 K_2 . \qquad (3\text{-}13)$$

Comparing (3-11) and (3-13), it shows that the minimal area allocation is achieved when A_C equals to A_R. Note that this optimal area allocation is again independent of constrains K_1 and K_2.

3.2.3 Single Pole Active Filter with Transconductance Networks

The previous filter structure requires a big component ratio to achieve large dc gains. This big component ratio invariably requires a large area to realize the large resistor. Since the feedback resistor in the previous filter simply serves as a “Transconductance” element, the issue of maintaining the same overall transfer function with lower component ratios using alternative transconductance elements deserves attention. A modification of this first order filter using a T-network to replace the resistor will reduce the area dramatically while keeping very good linearity [1]. The modified networks are shown in Figure 3-3.and Figure 3-4.

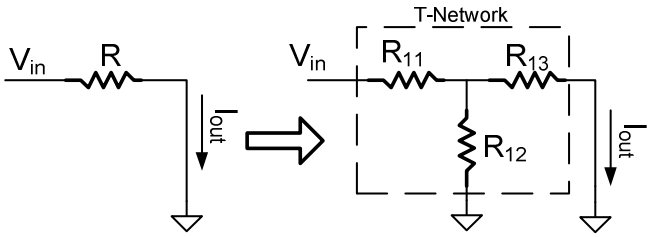

Figure 3- 3 -- Single Resistor Replaced by T-network.

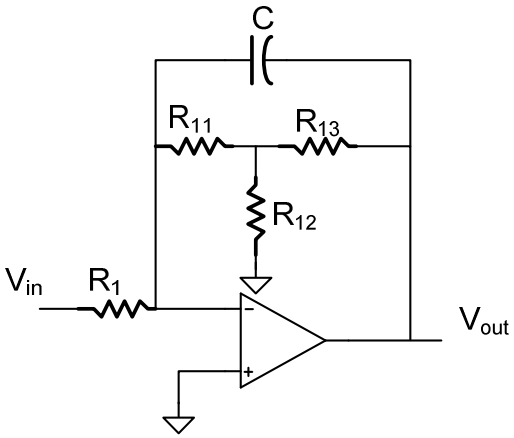

Figure 3- 4 -- First Order Active Filter with T-network.

The relationship between the resistor R_2 and the corresponding resistors of the T-network is given by the expression:

$$R_2 = \frac{R_{21}}{R_{22}} R_{23} + R_{21} + R_{23}. \qquad (3\text{- }14)$$

If R_{22} is sufficiently small, equation (3-14) can be reduces to the approximate relationship:

$$R_2 \cong \frac{R_{21}}{R_{22}} R_{23}. \qquad (3\text{- }15)$$

For the appropriate values of R_{21}, R_{22} and R_{23}, a dramatic reduction in the area required to realize the overall "transconductance" R_2 can be achieved. To find the optimum area allocation for this circuit, observe there are now four resistor values and one capacitor values

with only two constraints, dc gain and pole frequency. We will now establish the 4 constraints by setting the ratio of R_{21} over R_{22} as K_3 and R_{21} over R_{23} as K_4:

$$\frac{K_3R_{23}+R_{23}+R_{21}}{R_1}=K_1, \tag{3- 16}$$

$$(K_3R_{23}+R_{21}+R_{23})C=K_2\ , \tag{3- 17}$$

$$\frac{R_{21}}{R_{22}}=K_3\ . \tag{3- 18}$$

$$\frac{R_{21}}{R_{23}}=K_4. \tag{3- 19}$$

Building the Hamiltonian function as below:

$$\begin{aligned} H\ =\ & A_T+\lambda_1(\frac{K_3R_{23}+R_{21}+R_{23}}{R_1}-K_1) \\ & +\lambda_2[(K_3R_{23}+R_{21}+R_{23})C-K_2]\ \cdot \\ & +\lambda_3(\frac{R_{21}}{R_{22}}-K_3)+\lambda_4(\frac{R_{21}}{R_{23}}-K_4) \end{aligned} \tag{3- 20}$$

Taking the partial derivatives of R_1, R_{21}, R_{22}, R_{23}, and C and set these equations to zero, we have:

$$\frac{\partial H}{\partial R_1}=\frac{1}{R_d}+\lambda_1(-\frac{K_3R_{23}+R_{21}+R_{23}}{R_1^2})=0\ , \tag{3- 21}$$

$$\Rightarrow \frac{R_1}{R_d}=\lambda_1\frac{K_3R_{23}+R_{21}+R_{23}}{R_1}=\lambda_1K_1, \tag{3- 22}$$

$$\frac{\partial H}{\partial R_{21}}=\frac{1}{R_d}+\lambda_1(\frac{1}{R_1})+\lambda_2(C)+\lambda_3(\frac{1}{R_{22}})+\lambda_4\frac{1}{R_{23}}=0\,, \tag{3- 23}$$

$$\Rightarrow \frac{R_{21}}{R_d}=-\lambda_1\frac{R_{21}}{R_1}-\lambda_2R_{21}C-\lambda_3K_3-\lambda_4K_4\,, \tag{3- 24}$$

$$\frac{\partial H}{\partial R_{22}} = \frac{1}{R_d} - \lambda_3 (\frac{R_{21}}{R^2_{22}}) = 0\,, \tag{3- 25}$$

$$\Rightarrow \frac{R_{22}}{R_d} = \lambda_3 \frac{R_{21}}{R_{22}} = \lambda_3 K_3\,, \tag{3- 26}$$

$$\frac{\partial H}{\partial R_{23}} = \frac{1}{R_d} + \lambda_1 (\frac{1+K_3}{R_1}) + \lambda_2 (1+K_3) C - \lambda_4 \frac{R_{21}}{R_{23}^2} = 0\,, \tag{3- 27}$$

$$\Rightarrow \frac{R_{23}}{R_d} = -\lambda_1 \frac{(1+K_3) R_{23}}{R_1} - \lambda_2 (1+K_3) R_{23} C + \lambda_4 K_4\,. \tag{3- 28}$$

From constrains (3-16) and (3-17), we can derive:

$$(1+K_3) R_{23} = K_1 R_1 - R_{21}\,, \tag{3- 29}$$

$$(1+K_3) R_{23} = \frac{K_2}{C} - R_{21}\,. \tag{3- 30}$$

Replacing (3-29) and (3-30) into the equation (3-28), we have:

$$\frac{R_{23}}{R_d} = -\lambda_1 K_1 + \lambda_1 \frac{R_{21}}{R_1} - \lambda_2 K_2 + \lambda_2 R_{21} C + \lambda_4 K_4\,. \tag{3- 31}$$

It is very obviously that:

$$A_R = (22) + (24) + (26) + (31) = -\lambda_2 K_2\,. \tag{3- 32}$$

$$\frac{\partial H}{\partial C} = \frac{1}{C_d} + \lambda_2 (K_3 R_{23} + R_{21} + R_{23}) = 0\,. \tag{3- 33}$$

$$A_C = \frac{C}{C_d} = -\lambda_2 (K_3 R_{23} + R_{21} + R_{23}) C = -\lambda_2 K_2\,. \tag{3- 34}$$

It clearly shows that the conjecture presented above is true for the first-order filter with the T-network and it will reduce the passive area further. Now the question is if that is the truth for alternate structure for higher order filters? The following part is focused on the several most popular second-order filters.

3.3 Optimum Area Allocation for Second Order Filters

Three second-order filters will now be presented in this section. These are the Tow-Thomas Biquad, the Tow-Thomas Biquad with T-networks to reduce component spread, and the bridged-T feedback structure. The Tow-Thomas Biquad and the bridge-T feedback structures have been widely used for implementing analog filters. The modified Tow-Thomas Biquad is used for building high-linear integrated audio frequency filters within fairly small area [2]. These structures were chosen because they use different numbers of passive components, have different component rations, and use different numbers of op amps.

3.3.1 Tow-Thomas Biquad

The first structure for inspecting is Tow-Thomas biquad.

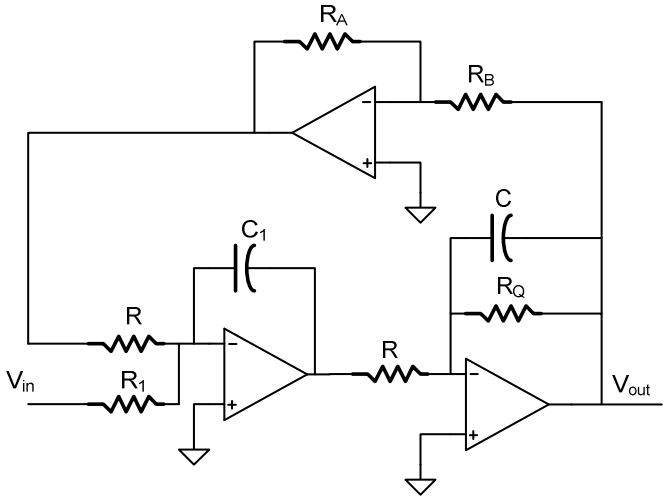

Figure 3- 5 -- Tow-Thomas Biquad.

The transfer function is shown as below:

$$\frac{V_o}{V_i} = \frac{\left(\frac{R}{R_1}\right)\cdot\left(\frac{1}{R^2CC_1}\right)}{s^2 + \frac{s}{R_Q C} + \frac{1}{R^2CC_1}}. \qquad (3\text{- }35)$$

$$A_T = A_R + A_C = \frac{2R + R_1 + R_Q}{R_d} + \frac{C_1 + C}{C_d}. \quad (3\text{-}36)$$

In this implementation, we have assumed the integration resistors are equal. We will not consider any resistor area associated with the resistors used to realize the finite gain amplifier, that is, the area required to realize the two R_A resistors will be ignored. We will ignore these resistors because we view this as a dimensionless gain block. Thus, we will consider the area related with the components that determine the poles of the network, specifically the two R resistors, the R_Q resistor and the capacitors C and C_1. If the w_0, Q and dc gain are all set, we have three constrains:

$$R_Q C = K_1, \quad (3\text{-}37)$$

$$R^2 C C_1 = K_2, \quad (3\text{-}38)$$

$$\frac{R}{R_1} = K_3. \quad (3\text{-}39)$$

Following the same analysis in previous section, we building the Hamiltonian function:

$$H = A_T + \lambda_1(R_Q C - K_1) + \lambda_2(R^2 C C_1 - K_2) + \lambda_3(R - K_3 R_1), \quad (3\text{-}40)$$

Taking the partial derivatives of R, R_1, R_Q and C, we can get the expression of the area for resistors and capacitors respectively:

$$A_R = \frac{2R}{R_d} + \frac{R_1}{R_d} + \frac{R_Q}{R_d} = -2\lambda_2 K_2 - \lambda_1 K_1, \quad (3\text{-}41)$$

$$A_C = \frac{C}{C_d} + \frac{C_1}{C_d} = -2\lambda_2 K_2 - \lambda_1 K_1, \quad (3\text{-}42)$$

Comparing the equations (3-41) and (3-42), we can see that the area of resistors is the same as the area of capacitors when minimum passive area is obtained. This results is still independent of constrain K_1, K_2, K_3.

3.3.2 Tow-Thomas Biquad with the Transconductance T-network

After the transconductance network has been introduced into the circuit, all the large resistors are replaced by T-networks [2]. R, R_1, R_Q in Figure 3-5 are all replaced by the T-networks composed by three resistors, R_1, R_2 and R_3 with the relationship: $R \cong \frac{R_1}{R_2} \cdot R_3 = KR_3$.There is similar transformation and all the analysis is the same as the first-order one presented in section 3.2. From that, we know that this conjecture is still hold in the second-order filters with T-network. Thus this strategy shows practical importance in the design of the RC-filters for audio frequency applications.

3.3.3 Second-order Bridge-T Feedback

Another popular second-order system is studied in this section.

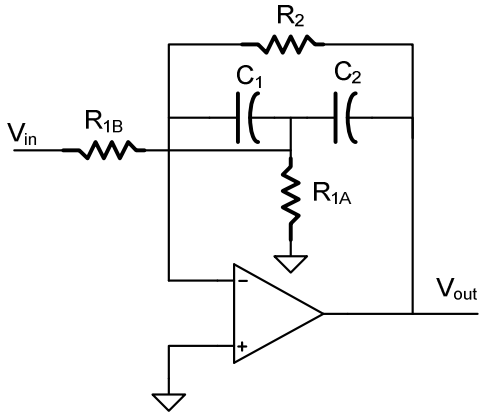

Figure 3- 6 -- Second-Order Bridge-T Feedback Circuit

The transfer function is given below:

$$T(s) = \frac{\frac{1}{R_{1B}C_2}S}{S^2 + S\frac{(C_1 + C_2)}{R_2C_1C_2} + \frac{(R_{1A} + R_{1B})}{R_{1A}R_{1B}R_2C_1C_2}}. \qquad (3\text{- }43)$$

Three constrains are set:

$$\frac{C_1 R_2}{R_{1B}(C_1 + C_2)} = K_1, \tag{3- 44}$$

$$\frac{(R_{1A} + R_{1B})}{R_{1A} R_{1B} R_2 C_1 C_2} = K_2, \tag{3- 45}$$

$$\frac{(C_1 + C_2)}{R_2 C_1 C_2} = K_3 \tag{3- 46}$$

Total area and Hamiltonian function are given as below:

$$A_T = \frac{R_2 + R_{1A} + R_{1B}}{R_d} + \frac{C_1 + C_2}{C_d}, \tag{3- 47}$$

$$\begin{aligned} H = A_T &+ \lambda_1 [\frac{C_1 R_2}{R_{1B}(C_1 + C_2)} - K_1] + \lambda_2 [\frac{(R_{1A} + R_{1B})}{R_{1A} R_{1B} R_2 C_1 C_2} \\ &- K_2] + \lambda_3 [\frac{(C_1 + C_2)}{R_2 C_1 C_2} - K_3] \end{aligned}. \tag{3- 48}$$

Take the partial derivatives of *H* respect to all the variables to achieve the following results.

$$A_R = \frac{R_{1A} + R_{1B} + R_2}{R_d} = 2\lambda_2 K_2 + \lambda_3 K_3, \tag{3- 49}$$

$$A_C = 2\lambda_2 K_2 + \lambda_3 K_3. \tag{3- 50}$$

Comparing the equation (3- 51) and (3- 52), it proves that the area for resistors equates the area of the capacitors when the optimum passive area is achieved.

3.4 Other Active Filter Structures

The first-order and second-order filter structures studied in the previous two sections represent some of the more popular first-order and second-order active RC filters. Although they are of interest in their own right, they were also selected because they represent

fundamentally different filter architectures with varying numbers of components, component spreads and internal nodes. Since the minimum total area for the resistors and capacitors was always achieved when the total resistor area equaled the total capacitor area, the question about whether this is a property inherent in all active RC filters naturally arises. Needles to say, when the authors investigated this problem, essentially all active filters that were considered, with the exception associated with the resistors needed to build finite gain amplifiers as described below, possessed this property. Thus, it is conjectured that this property is shared by a much larger number of useful active RC filters. The exception has to do with circuits that use resistors to build finite gain amplifiers. The Tow-Thomas biquad discussed above included such a finite gain amplifier as do some of the Sallen and Key filters. Beyond observing that such filters are characterized by a hinged graph of passive components in contrast to all examples considered in the previous sections in which the graph of passive components are not hinged, we will not attempt to conjecture what topological properties of the filter are necessary for the equal resistor/equal capacitor area property to hold.

3.5 Conclusion

The problem of minimizing area for passive components in audio frequency active filters has been addressed for the first time in closed-form. In this paper, several popular first-order and second-order RC active filter structures with substantially different component ratios and with varying numbers of passive components were considered. These structures are all inherently continuous-time in nature and offer excellent linearity when compared to alternative continuous-time monolithic filter approaches based upon using transconductance

networks or MOSFETs as resistance or transresistance elements. A detailed analysis of each of these structures showed that the total area for the resistors and capacitors is minimized when the total resistor area equals the total capacitor area irrespective of capacitance density, resistance density, pole locations or DC gain.

3.6 References

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CHAPTER 4 LINEAR CURRENT DIVISION CIRCUIT PRINCIPLE STUDY AND A NOVEL CURRENT DIVIDER DAC DESIGN

Abstract-this chapter presents the study of a well established current division circuit, which has been claimed inherently linear and referenced frequently in publications. Various of reported works have used this current division circuit as their basic building blocks for its high linearity and the simple circuit structure including the data conversion circuits, signal filtering circuit, precision gain control blocks, etc. Understanding the advantages and, even more important, the limitations of this technique would benefit the further exploiting of potential applications. Analytic study provides the close form expressions with certain approximation shows highly agreements with the original statement that this structure is inherently linear and its linearity is independent of the electrical variables and only relies on the transistors geometrical match performance. However, the more accurate study with simulation results suggests that there are limitations for using this technique in terms of high linearity in the most popular semiconductor processes. The exploration of more general circuit principle provides the explanation of the successful linearity implementations of this current division circuit in wide range of applications. Besides the limitation of this technique, the further study exploits the potential benefit with moderate linearity and extreme simple structure for low resolution, low power and compact DAC design. Based on these advantages, a novel 8-bit DAC structure has been introduced in the following section. A dummy string has been brought into this DAC to significantly increase the operating speed with very slightly cost of the active area. Also a segment structure has been adopted due to directly current summing nature to further reduce the occupied area and the power consumption. With the potential applications, a 6-bit and 8bit DAC has been built. The

output stage has been design to be followed by a buffer or drive kilo ohm resistive load directly. With the dummy string, this current division DAC can also provides the fully differential output. After the circuit design and layout, the total active area for 8-bit DAC is only 100 um x 100 um in standard TSMC 0.18 um CMOS process with very relax digital circuitry layout. The simulation results demonstrate the peak DNL about 0.8 LSB and INL at 0.5 LSB. Also this DAC offers superior dynamic linearity that the SFDR only drop one dB at around 58 dB with the input signal approaching at the Nyquist rate operating with 200 MHz update rate.

4.1 Introduction

Before the analysis of this current division started, a general definition of current divider is introduced here. Although there is no strict definition eve being reported, a standard current divider circuit is shown in Figure 4-1(a) according to our common wisdom. In this current divider, part of the input current passes through one sub-circuit and the balance passes through a second sub-circuit. If ideal, it will provide a branch current in one sub-circuit, I_1, which is a fixed fraction of the total input current, I_{IN}. In this case, the branch current can be expressed as (4-1):

$$I_1 = \theta I_{IN}, \tag{4- 1}$$

where θ is the division factor and it is independent of I_{IN} or any other electrical variables applied on the circuit. Accurate and linear current division circuits are widely required in the design of data converters, analog filters and a host of other applications. The simplest basic current divider circuit is that obtained by replacing C_{kt1} and C_{kt2} in Figure 4-1(*a*) with resistors. Circuits that have some of the properties of the basic current divider have also been

called “current dividers” [1] although the exact definition of more general current dividers are not well-established. Two circuit structures that share some of the same properties of the basic current divider are shown in Fig. 1b and Fig. 1c. In the more general current divider of Fig. 1b, it may not be possible to partition the current divider into two distinct subcircuits but the partitioned sourcing currents entering the current divider will remain as partitioned sinking current exiting the current divider as shown in the figure. In an even more general current divider, the partitioned sourcing currents may not be available as sinking currents and the current will only be divided at the output end. This situation is depicted in Fig. 1c. In this paper, the definition of “current divider” will be relaxed defined and then any format shears with those three definitions will be considered as a current divider circuit.

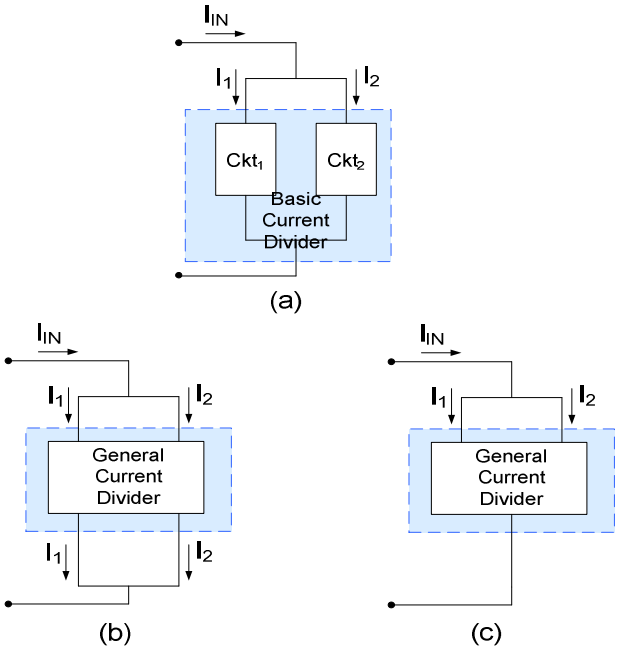


Figure 4- 1-- General Formats of Current Division Circuits.

In 1992 Bult and Geelen [1] introduced an interesting and simple two-transistor current divider and claimed it to be “inherently linear” with a current division factor θ that was dependent only upon the devices geometries ratio. In addition to its small size and simple

structure, the authors observed that this divider is attractive because the attenuation factor can be accurately controlled in most modern semiconductor processes. For the nomination convenience, the circuit shown in Figure 4-2 will be denominated as the Bult-Geelen divider circuit, presented in [1], shown in Figure 4-2.

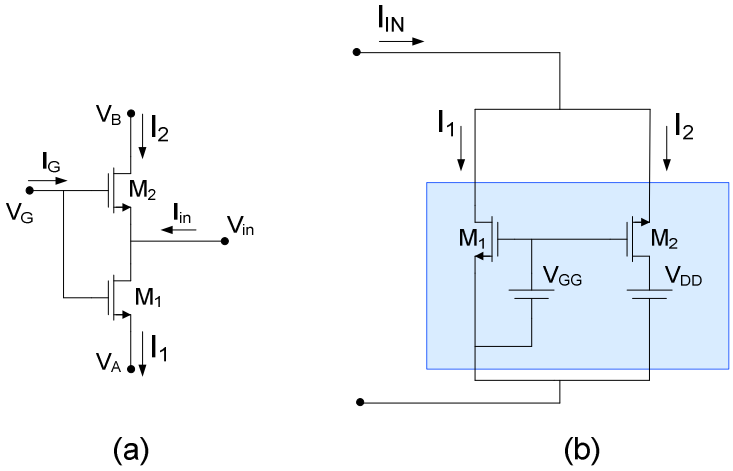


Figure 4- 2 -- Inherently Linear Current Divider [1].

This structure has been influential in the development of diverse of analog circuit including the digitally programming current division block used in MOSFET-only ADC converter [2]-[4], a baseband channel-select filter for multi-standard wireless receiver [5]-[7], digitally tuning analog filters [8]-[13], variable gain current amplifier [14]-[20] and current conveyors [21]-[28] , memory and sensor design [29]-[36] and several other applications [37]-[46].

All above works have reported phenomenal linearity performance based on this current divider with inherently linearity: the THD of a volume control circuitry [1] was better than -85 dB, the THD of a 10-bit A/D [2] converter was -79dB, and a channel-select filter [5] built around this structure achieved -80~-94 dB spurious free dynamic range (SFDR). These

linearity measures, all experimentally verified, are very impressive considering that the critical and basic parts of these circuits are derived from small MOS transistors configured as simple two-transistor current dividers shown in Fig. 2 (a) rather than with large passive components. The further exploration of this simple but linear current divider will benefit the potential applications for any high linear circuits.

However, the following study presented in this paper will demonstrate that this Bult-Geelen current divider didn't exploit the linearity of this simple two-transistor circuit divider but rather exploit somehow more general electrical circuit principles.

4.2 Close Form Analysis of the Current Divider

Although this current divider has been reported with inherently high linearity, no analytical proves have been actually presented. The close form expression of this linear current division property will be of particular interested with the complexity that manual analysis can handle. In this section, the square-law model will be used for derive the sink current relationship with the input current.

The two-transistor current divider in Figure 4-2 can be considered as a 4-terminals network. If the voltages of the terminals $\{V_{GA}, V_{BA}, V_{inA}\}$ have been chosen as the independent variables here, the currents flow out of the terminals $\{I_G, I_{IN}, I_1\}$ are naturally become dependent variables. It is easily to prove that two transistors can work in two different cases; M_1 and M_2 are both in the triode region or M_1 is operating in the triode region while M_2 operates in saturation region. If assume two transistors have the same threshold voltages and the finite output impedance is ignored, with basic square-law models, the electrical variables of this 4-terminal device are related as (4-2)-(4-4):

$$I_G = 0, \tag{4- 2}$$

$$I_1 = \eta_1\left(V_{GA} - V_T - \frac{V_{inA}}{2}\right)V_{inA}, \tag{4- 3}$$

$$I_{in} = \eta_1\left(V_{GA} - V_T - \frac{V_{inA}}{2}\right)V_{inA} - \eta_2\left(V_{Gin} - V_T - \frac{V_{BA} - V_{inA}}{2}\right)(V_{BA} - V_{inA}), \tag{4- 4}$$

where, V_T is the threshold voltage, $\eta_1=\mu C_{OX}(W_1/L_1)$, and. $\eta_2=\mu C_{OX}(W_2/L_2)$. The branch voltages are defined as $V_{GA}=V_G-V_A$, $V_{BA}=V_B-V_A$, and $V_{inA}=V_{in}-V_A$. The current-divider properties are not apparent from this formulation. If the mixed port variables $\{I_{in}, V_{GA}, V_{BA}\}$ are selected as the independent variables and thus $\{I_G, I_1, V_{inA}\}$ will be the dependent variables, it follows from a tedious but straightforward analysis that the device can be equivalently modeled by (4-5)~(4-7);

$$I_G = 0, \tag{4- 5}$$

$$I_1 = \left[\frac{\eta_1}{\eta_1 + \eta_2}\right]I_{in} + \frac{\eta_1\eta_2}{\eta_1 + \eta_2}V_{BA}\left(V_{GA} - V_T - \frac{V_{BA}}{2}\right), \tag{4- 6}$$

$$V_{inA} = V_{GA} - V_T - \sqrt{(V_{GA} - V_T)^2 - 2\left(\left[\frac{1}{\eta_1 + \eta_2}\right]I_{in} + \frac{\eta_2}{\eta_1 + \eta_2}V_{BA}\left(V_{GA} - V_T - \frac{V_{BA}}{2}\right)\right)}, \tag{4- 7}$$

For the second cases that the M_1 works in the triode region and M_2 operates in the saturation region, the same analysis has been carried out and this 4-terminal device behavior in the following equations:

$$I_G = 0, \tag{4- 8}$$

$$I_1 = \left[\frac{\eta_1}{\eta_1 + \eta_2}\right]I_{in} + \frac{\eta_1\eta_2}{2(\eta_1 + \eta_2)}(V_{GA} - V_T)^2, \tag{4- 9}$$

$$V_{inA} = (V_{GA} - V_T)\left(1 - \sqrt{\frac{\eta_1 - \frac{2I_{in}}{(V_{GA} - V_T)^2}}{\eta_1 - \eta_2}}\right), \quad (4\text{- }10)$$

If this two-transistor circuit is treated as a current divider according what we defined in Figure 4-1, the current division factor is determined by the ratio of certain sink current over the total incoming current. With the focus on (4-6) and (4-9), it is clearly that with certain circuitry settings, for example, choosing V_{BA} equals to zero in (4-6) and pick the value of V_{GA} equals to the V_T in (4-9), the current I_1 will only be determined by the first term of those two equations by a simple coefficient:

$$\theta_{TT} = \frac{\eta_1}{\eta_1 + \eta_2}. \quad (4\text{- }11)$$

With the assumptions mentioned above, (4-11) is unchanged with the M_2 transistor shifting between the saturation region and the triode region. If inserting the expressions of η_1 and η_2 into (4-11) and representing the current division factor θ_{TT} in forms of the geometrical ration, the following equation is derived:

$$\theta_{TT} = \frac{\eta_1}{\eta_1 + \eta_2} = \frac{1}{1 + \left(\frac{L_1}{L_2}\right)\left(\frac{W_2}{W_1}\right)} \underset{L_1 = L_2}{=} \frac{W_1}{W_1 + W_2}. \quad (4\text{- }12)$$

The accuracy of θ_{TT} is determined by the geometrical ratio of two transistors and it is well controlled in the most modern CMOS process. Therefore, the current division accuracy is almost guaranteed within the same level of the dimension match performance in certain process. This is what called the inherently linear because θ_{TT} is independent of any other electrical variables.

However, by comparing (4-6) and (4-9) with the ideal current divider equation of (4-1), some significant differences does appears. The first distinction is that in whatever circuit this current divider is embedded, the voltages V_{GA} and V_{GB} must not depend upon I_{in} if the linear current division property is to be maintained. The second one is the assumption mentioned in the previous part to make the second term omitted and otherwise offset part will rise and this offset is dependent on the terminal voltages. The third incompatibility is the concern that unless the circuit is driven at the input node with a current source with infinite output impedance, the change in the voltage V_{inA} will finite output impedance of the current source will modulate the current I_{in} and thus introduce certain voltage dependence and cause the nonlinear relationship between the I_1 and I_{in}. If all these conditions are appropriately managed, the current divider is perfectly linear and its accurate is only limited by the match potential in a certain process in which the simple square-law model accurately predicts the performance of the MOS transistor.

Unfortunately few if any processes in use today are accurately characterized by the simple square law model. As reported in [1], when a more accurate model is used, model-dependent nonlinearities will be introduced. An appreciation for the circuit performance and limitations as affected by a more accurate MOSFET model and an understanding of the limitations inherent in the architecture will now be developed. In particular, we will focus on accuracy and linearity of the current divider.

4.3 Accuracy and Linearity Coefficients Definition

Before more accurate models are used to study the limitations and accuracy of the linearity of this current divider, two coefficients would be established in the following part to evaluate this current divider in difference applications.

4.3.1 Accuracy Definition

The first interesting property with this current divider is that how accurate the real current ratio compared with the theoretical prediction given by the (6) and (9). The division factor of the current divider in the presence of a better device model will be defined as:

$$\theta_{TTACT} = \left.\frac{\partial I_1}{\partial I_{in}}\right|_{\{I_{inQ}, V_{GAQ}, V_{inAQ}\}}, \tag{4- 13}$$

and the division factor accuracy, in percent, will be defined as:

$$\gamma = \left[\frac{\theta_{TT} - \theta_{TTACT}}{\theta_{TT}}\right] \times 100\% . \tag{4- 14}$$

This parameter will describe the accuracy of the current divider with the quiescent input current.

4.3.2 Linearity Definition

Two different definition of linearity will be defined here because according to difference applications either one or both are of interested. The first one is based upon the deviation of the transfer characteristics of the attenuated current from a referenced straight line. Very similar with the definition of INL in data converter circuit, this linearity implies the linearity of this current divider with a slow varying input signal. The second one is based upon

the spectral performance of the output current with the presence of a sinusoidal excitation. By using the actual attenuation factor derived from (4-13), the gain error will be compensated and this calibrated fit line can be expressed as:

$$I_{1FIT}(I_{in}) = I_{1Q} + \left.\frac{\partial I_1}{\partial I_{in}}\right|_{\{I_{inQ}, V_{GAQ}, V_{inAQ}\}} \cdot (I_{in} - I_{inQ}), \tag{4- 15}$$

Referenced to the fit line, the linearity then can be found by using the equation below:

$$\Delta = \left[\frac{I_1(I_{in}) - I_{1FIT}(I_{in})}{I_{1FIT}(I_{in})}\right] \cdot 100\%, \tag{4- 16}$$

where I_{1Q} is the current I_1 at the quiescent value of the input current, I_{inQ}.

The second linearity quality is evaluated with fast varying input signal usually described by spectrum performance. The spectral performance will be defined in terms of the total harmonic distortion (THD) of the time-varying part of I_1 in the presence of a sinusoidal input current. In our study, both definitions of linearity show certain extend of dependent upon the magnitude of the input current with the nonlinearity going to zero as the deviation of the input current from the quiescent value goes to zero. We will define a full-scale input current to be I_{1Q}/θ_{TT}. If the transistor M_2 is operating in the saturation region when I_{IN}=0, the full-scale input current will be the current that causes M_2 to leave strong inversion and represents the maximum input current for current divider. If the transistor M_2 is operating in the triode region, when I_{IN}=0, the full-scale input current does not represent an upper bound on the input current and can just be viewed as a reference current level.

4.4 More Accurate Model Analysis and Simulations

Reminded from the section II, several simplifications have been made to achieve the final close form expressions including identical threshold voltages, ignoring the finite output impedance of the transistors, second order effects and the substrate effect, etc. Those simplifications are not valid in more accurate model analysis and the real performance of the current divider will only be predicted with a more accurate model of devices used in current processes so that higher level model analysis becomes necessary. An analytical analysis with a more accurate device model becomes unwise but a computer simulation is useful and considerably accurate for developing an appreciation for the linearity and accuracy attainable with the current divider. Simulations will be based upon the circuit of Figure-2(b) where the terminal voltages V_{DD} and V_{GG} are fixed. BSIM device models for the TSMC 0.35μm and the TSMC 0.18μm processes will be used for those simulations.

In order to verify the linearity and its dependence upon all kinds of circuit characterizations, the simulations are set up with as many different circuit properties as possible. The simulation corners include large and small devices sizes, large excess bias ($V_{EB}=V_{GSQ}-V_T$) voltage and small one, single-region and two-region operations of the transistors M_1 and M_2, and large feature size and small feature size processes. The accuracy of an attenuator designed for an attenuation factor of $\theta_{TT}=0.5$ for long devices is shown in Table 4-1. From this table it can be observed that the accuracy of the attenuation factor is quite limited unless the operation of both devices is restricted to the triode region when large excess bias voltages are used.

Table 4- 1 Accuracy of the Current Divider for Different Cases.

V_{DD} (V)	V_{GG} (V)	V_{EB} (V)	W_1 (um)	W_2 (um)	L_1 (um)	L_2 (um)	Process	Q-Point Ope.		θ_{TT}	θ_{TTACT}	γ (%)
								M1	M2			
1.1	1.1	0.23	12	12	4	4	0.35	Triode	Sat	0.5	0.476	-4.8
1.65	1.65	2.79	12	12	4	4	0.35	Triode	Sat	0.5	0.491	-1.8
0.2	1.2	0.303	12	12	4	4	0.35	Triode	Triode	0.5	0.491	-1.8
0.2	1.65	2.79	12	12	4	4	0.35	Triode	Triode	0.5	0.5	0
0.9	0.9	0.125	6	6	2	2	0.18	Triode	Sat	0.5	0.476	-4.8
1.8	1.8	1.34	6	6	2	2	0.18	Triode	Sat	0.5	0.483	-3.4
0.1	0.9	0.225	6	6	2	2	0.18	Triode	Triode	0.5	0.495	-1
1.8	1.8	0.898	6	6	2	2	0.18	Triode	Triode	0.5	0.493	-1.4

The linearity of the current divider will be testified with the similar strategy. Different sizes of the transistors, different bias voltage levels and different feature size processes are simulated and simulation results are shown in Figure 4-3~Figure 4-6.

The static nonlinearity represented in forms of the deviation is shown in Figure 4-3 and Figure 4-4 for TSMC 0.35 um process and TSMC 0.18 um process, respectively. In these plots, “TT” and “TS” represent two kinds of the operation regions scenarios for M_1 and M_2. “TT” implies M_1 and M_2 are both in triode region and “TS” represents one in triode while the other one in saturation. The term “HVeb” and “LVeb” are the abbreviations of the different bias voltage levels with “large excess bias voltage (overdrive voltage)” and “low excess bias voltage (overdrive voltage)”.

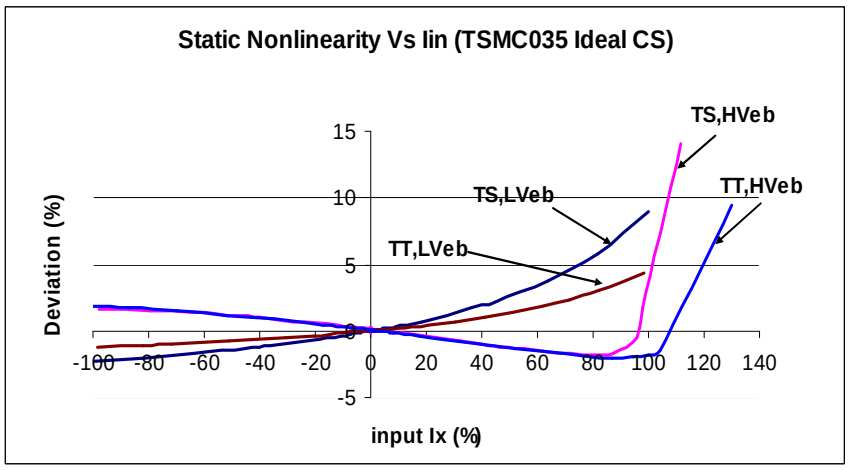


Figure 4- 3 -- Static Nonlinearity in TSMC035 Process.

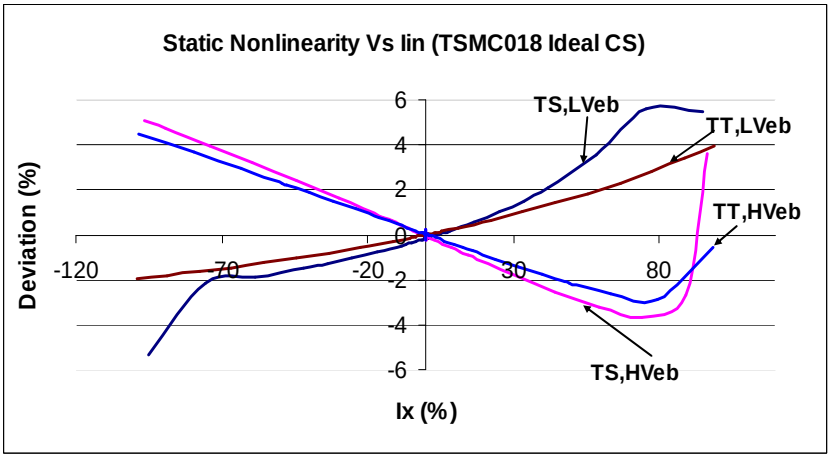


Figure 4- 4 -- Static Nonlinearity in TSMC018 Process.

From Figure 4-3 and Figure 4-4, it is clearly shown that the linearity will get worse with the increasing input current magnitude and this static linearity is very limited for even moderate magnitude of the input current with noticing that the deviation ranges from 3% to 5% when the input current approaching to about 50% of the full range. Also this static nonlinearity certainly shows some dependency upon the biasing level and the operation regions of the transistors. It is interesting to observe a consistent phenomenon that, in both two processes, the best linearity performances are associated with the case that two transistors

are both in the triode region with large V_{EB} voltages are applied. Recalling the best accuracy performance in the Table 1, it is very interesting to notice that the current divider will achieve the best accuracy with two triode region operating transistors with large V_{EB}. The transistor will behavior as a resistor when it is operates in deep triode region and thus it will provide the high linearity according to the simulation discussed above and it indicated that all the transistors in the current divider are preferred to work in the deep triode region when static or low frequency linearity is important.

The spectrum performance will be shown in Figure 4-5 and Figure 4-6 below.

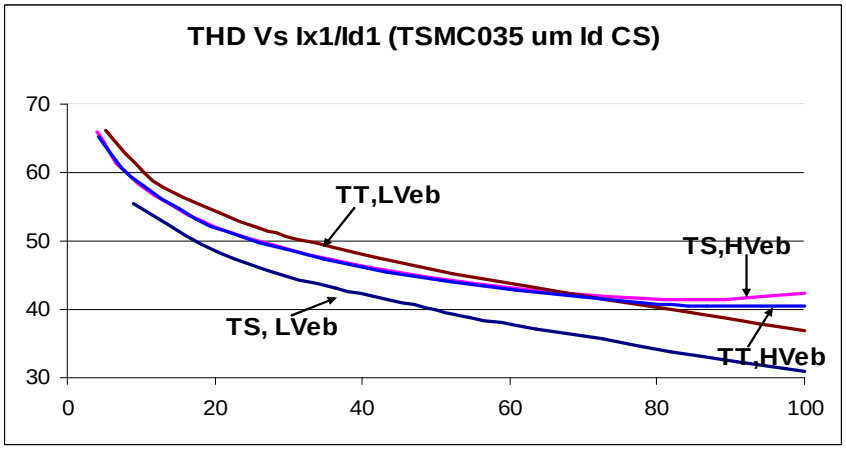


Figure 4- 5 -- Dynamic Nonlinearity in TSMC035 Process.

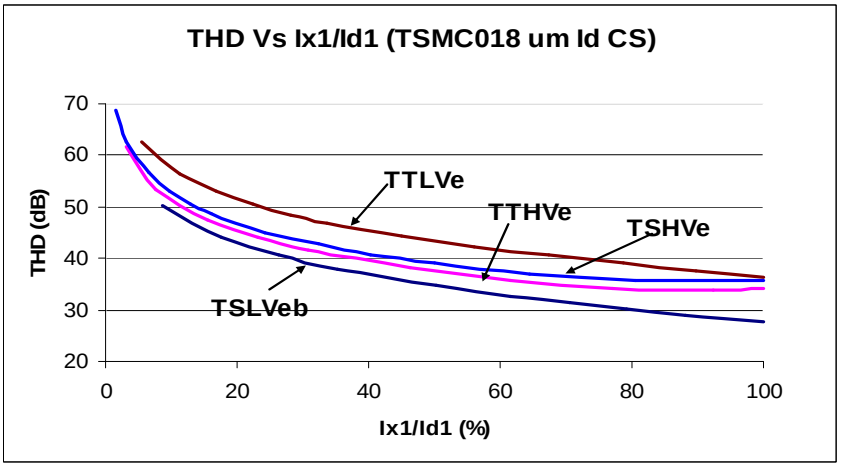


Figure 4- 6 -- Dynamic Nonlinearity in TSMC018 Process.

The THD performance again exhibits that the linearity of this current divider is a strong function of the input current amplitude and also dependent on the device size, biasing level and the different process. The THD will limited to about 30~40 dB level if reasonable input current level is expected. The best linearity occurs when the two transistors are both in the triode region with low level V_{EB}. This is because the harmonic distortions are representative to the nonlinearity caused by the large input signal and the large V_{EB} will correspondingly result the larger current level than small V_{EB} with the same device size ratio.

Although many others different simulations have been done to explicitly exploit the linearity of this current divider including the minimum length devices, non-ideal input current sources and non-even current division ratios ($\theta_{TT} \neq 0.5$), the results will not be presented here due to the volume limitation and similarity. All the simulations exhibit the limited linearity with real design models and also show the dependence of linearity upon the device size, biasing level, operation region and the processes technology.

After the conclusive study to show that the current divided introduced by [1] is quite limited and also dependents upon numbers of electrical variables. The successful implementation of really high linear circuits based on this current divider in those published works must exploit some other general circuit principles and this topic will be discussed in the following section

4.5 Linear Current Division Principle

The conclusion from the last section seems to be conflict with all the experimental verified works. If the current divider circuit cannot provide enough linearity to achieve those phenomenal circuits, there must be some circuit principle to support those high linearity

designs. The study of this linearity principle will be addressed in this section. The current divider introduced by [1] and referenced in [2]-[46] as the fundamental building block is simplified as a single two-transistor pair and again shown below.

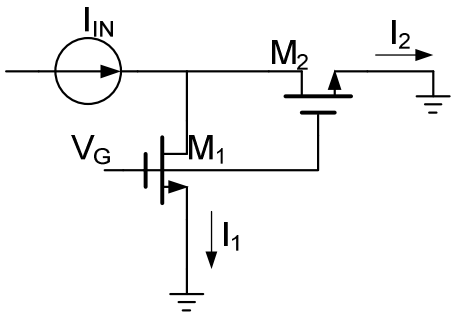


Figure 4- 7 -- Basic Current Division Cell used in [1]

This basic current division cell have been used as the volume controller in [1], transistor-based R-2R ladder in [2]-[3], digital tuning circuit in [4]-[7] and all those works have been experimentally proved to be very linear. If those two transistors are considered as identical, Figure 4-7 can be simplified as a more general circuit as shown in Figure 4-8.

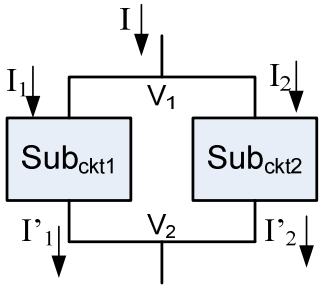


Figure 4- 8 -- Generalized Current Division Diagram Block.

It is very obvious that Figure 4-8 is a symmetrical circuit and the high linearity actually rely on the symmetry rather than the current division characteristics. Although the symmetrical circuit has been recognized as very linear for a long time, the linearity of Figure 4-8 will be discussed in the following part for the intact of this paper.

Sub_ckt1 and Sub_ckt2 are identical for the symmetry property. Therefore, for choosing any independent variable, voltage or current, the transconductance or transresistance function should be the same. The transresistance function is chosen here for producing the analysis. Assume the transresistance function for Sub_ckt1 and Sub_ckt2 are given as $f_{T1}(.)$ and $f_{T2}(.)$, respectively. It is obviously that follows:

$$I_1 = f_{T1}(V_2)\,, \tag{4- 17}$$

$$I_2 = f_{T2}(V_2). \tag{4- 18}$$

Because $f_{T1}(.)=f_{T2}(.)$, we can find $I_1=I_2$. From Kirchoff law, $I=I_1+I_2$, so the ratio of I_1 or I_2 over I will be 0.5 and it is clearly shown that this current division ratio is perfectly linear and independent of the transfer function of those Sub_ckts. Also this concept can be extended to any number of symmetrical branches as shown below:

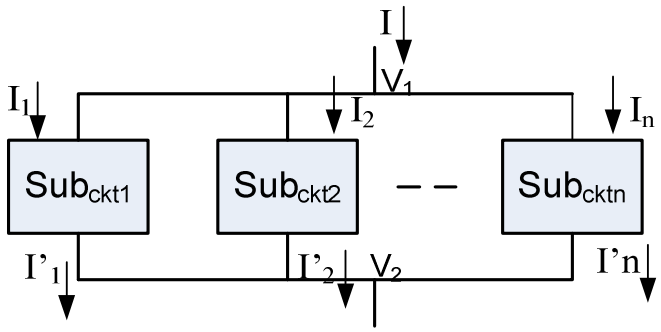


Figure 4- 9 -- Generalized Current Division Diagram Block with Multiple Current Sinks.

Similar as the analysis above, each branch current will have the same transresistance function: $f_{T1}(.)=f_{T2}(.)=\ldots=f_{Tn}(.)$. And all the current will be the same $I_1=I_2=\ldots=I_n$. By using the superposition, the ratio of any kind of combination of I_n over input current I will be pretty constant and this fixed current division ratio is also independent of any transfer function of each sub_ckt as long the symmetry is maintained. However, if the connection of the network

is asymmetrical and is shown as in Figure 4-10, the current ratio will not be guaranteed to be linear.

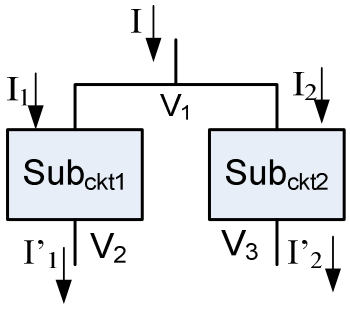


Figure 4- 10 -- Generalized Asymmetrical Current Divider Cell.

Now the current of each sub_ckt is then given:

$$I_1 = f_{T1}(V_2)\,, \tag{4- 19}$$

$$I_2 = f_{T1}(V_3)\,. \tag{4- 20}$$

The current of each sub_ckt is not the same again. The ratio of input current and any sink current is then the function of the transfer function of each such circuit and also the function of the node voltages. The circuit shown in the Figure 4-10 will not be perfectly linear.

The linearity of the symmetrical circuit is actually the fundamental principle that supported all the high linearity circuits for using this current division cell. In the next section, the exploiting of the real current divider will be presented.

4.6 A 8-bit Novel Low Power Compact Current Divider DAC Design

In the previous sections, the limitations of the linearity of the Bult-Geelen current divider have been addressed and the simulations exhibit conditional linear level with that two-transistor current division circuit. However, if a moderate linearity is tolerated in some applications, this current divider does show certain independency on the electrical parameters

besides its extreme simple structure and small area implementation. This independency can also be revealed from the close form analysis in section 4-2, in which, the current division factor θ_{TT} could be expressed as the function of only devices size ratios if other offset terms being managed properly with simple device models. Although the linearity of the continuous time input was really unacceptable, this current divider still shows potential usage if the input current is always at the DC level. Actually, almost all the design works based on this current divider applied it with constant input currents along with the symmetrical setting. The static linearity has been studied in section III, and with properly arranged design, the static linearity can achieved 6-8 bit level linearity. Therefore, a prototype of a low resolution, low power and very small area DAC is presented in this section.

With the bioelectronics devices getting more and more attentions, low power, small area, low price DAC is coming into the application engineers' sights. Usually, this type of DAC will provides 6-8 bits resolution and operates between ten of Kilo Hz to several Meg Hz range, but with very low power consumption and very small area [47]-[49]. Another important application for 8-bit level digital to analog conversion emerges from the fast revolution of high definition video systems [50]-[53]. The DAC in this kind of application are usually operates at hundreds of Meg Hz with 50-75 Ω resistive loads. 8-bit DAC also use the device compatible with microcontroller in data acquisition and control system, in which applications, the output buffer or high impedance is followed [54], [55]. One of the very interesting applications is combine the DAC with the filter for multiple communication standards transceiver design and this application is getting more attention with the fast growing market of the portable wireless communication devices [56]. The existing circuit structures for implementing 6-8 bit DAC are mostly R-2R resistor ladder and the current

string architecture For N-bit DAC, the current sources structure involve 2^N current source, which mainly limit the aggressively shrinking the total active area while R-2R structure uses much less number of components, however, the linearity strongly rely on the component mismatch and terminal voltage and thus the extra design effort was necessary to reduce the offset voltage appear at the two terminals [2]. This current division structure considerably simplifies the design by using very small number of components and it is also robust with the offset voltages at the terminals.

4.6.1 DAC Structure Develop

From section 4.2, the close form expressions of the output current in forms of the input current are given by (4-6) and (4-9). The same ideal can be expended to multiple transistors stack together. The three, four and k transistors current divider is shown below.

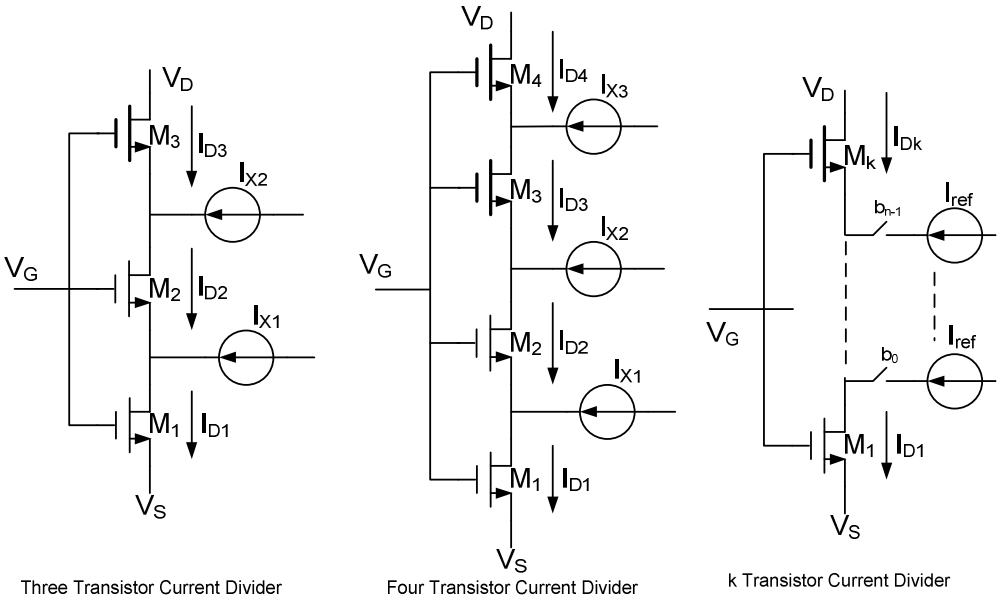


Figure 4- 11 -- Multiple Inputs Transistor Current Dividers Circuit.

The output current I_{D1} in the three transistor current divider can be expressed in the equations below with the two cases: all the transistors are in the triode region, as in (4-21) and the bottom ones operating in the triode region while the very top one in the saturation region, shown in (4-22).

$$I_{D1}=\frac{\eta_1\cdot\eta_2\cdot\eta_3}{\eta_1\eta_2+\eta_2\eta_3+\eta_1\eta_3}\cdot\frac{1}{2}V_{DS}(2V_{EB}-V_{DS})+\frac{\eta_1\eta_2+\eta_1\eta_3}{\eta_1\eta_2+\eta_2\eta_3+\eta_1\eta_3}I_{X1}+\frac{\eta_1\eta_2}{\eta_1\eta_2+\eta_2\eta_3+\eta_1\eta_3}I_{X2}. \quad (4\text{-}21)$$

$$I_{D1}=\frac{\eta_1\cdot\eta_2\cdot\eta_3}{\eta_1\eta_2+\eta_2\eta_3+\eta_1\eta_3}\cdot\frac{1}{2}V_{EB}^2+\frac{\eta_1\eta_2+\eta_1\eta_3}{\eta_1\eta_2+\eta_2\eta_3+\eta_1\eta_3}I_{X1}+\frac{\eta_1\eta_2}{\eta_1\eta_2+\eta_2\eta_3+\eta_1\eta_3}I_{X2}. \quad (4\text{-}22)$$

where, $\eta_i=\mu C_{OX}(W_i/L_i)$ and the I_{D1} can always be represented as the fraction of two input currents I_{x1} and I_{x2}. The similar equations can be derived for 4 transistor current divider shown in (4-23) and (4-24).

$$I_{D1}=\frac{\eta_1\cdot\eta_2\cdot\eta_3\cdot\eta_4}{\mathrm{Y}}\cdot\frac{1}{2}V_{DS}(2V_{EB}-V_{DS})+\frac{\eta_1\eta_2\eta_3+\eta_1\eta_3\eta_4+\eta_1\eta_2\eta_4}{\mathrm{Y}}I_{X1}+\frac{\eta_1\eta_2\eta_3+\eta_1\eta_2\eta_4}{\mathrm{Y}}I_{X2}+\frac{\eta_1\eta_2\eta_3}{\mathrm{Y}}I_{X3}, \quad (4\text{-}23)$$

$$I_{D1}=\frac{\eta_1\cdot\eta_2\cdot\eta_3\cdot\eta_4}{\mathrm{Y}}\cdot\frac{1}{2}V_{EB}^2+\frac{\eta_1\eta_2\eta_3+\eta_1\eta_3\eta_4+\eta_1\eta_2\eta_4}{\mathrm{Y}}I_{X1}+\frac{\eta_1\eta_2\eta_3+\eta_1\eta_2\eta_4}{\mathrm{Y}}I_{X2}+\frac{\eta_1\eta_2\eta_3}{\mathrm{Y}}I_{X3}. \quad (4\text{-}24)$$

where, $\mathrm{Y}=\eta_2\eta_3\eta_1+\eta_2\eta_3\eta_4+\eta_1\eta_3\eta_4+\eta_1\eta_2\eta_4$ and it is the function of devices size only. For the general case, the expression of output current when all the transistors working in the triode region is given in (4-25) and in (4-26), the top transistor is in the saturation region.

$$I_{D1}=\frac{1}{2}V_{DS}\cdot(2V_{EB}-V_{DS})\frac{\prod_{i=1}^{k}\eta_i}{D}+\sum_{i=1}^{k-1}I_{Xi}\cdot\frac{D-\sum_{p=1}^{i}\left(\prod_{j=1}^{k}\eta_j\Big/\eta_p\right)}{D}, \quad (4\text{-}25)$$

$$I_{D1} = \frac{1}{2} V_{EB}^2 \frac{\prod_{i=1}^{k} \eta_i}{D} + \sum_{i=1}^{k-1} I_{Xi} \cdot \frac{D - \sum_{p=1}^{i} \left(\prod_{j=1}^{k} \eta_j \Big/ \eta_p \right)}{D}. \quad (4\text{- }26)$$

Where, $D = \sum_{i=1}^{k} \left(\prod_{j=1}^{k} \eta_j \Big/ \eta_i \right)$.

From above analysis, it has proved that the current division principle will be valid when the multiple transistors stacking together. If purposely choosing all the transistors in the triode region and setting V_{DS} equals to 0, the output current can then be expressed as the function of the input currents with the division factors only dependent on the device size ratio. By carefully choosing the device size of each transistor, the output current can be expressed as the binary combination of the every input current and therefore the digital to analog function is realized. A 4-bit current mode DAC is shown below as an example:

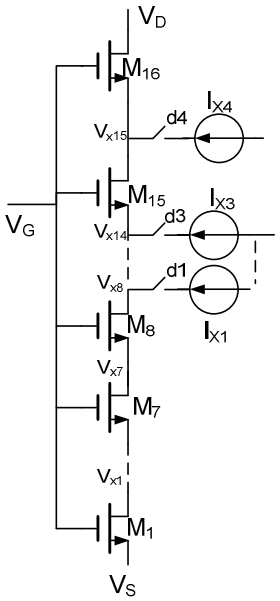


Figure 4- 12 -- 4-bit DAC based on Current Divider Principle.

There are total 16 transistors with the same size and 4 identical current sources in Figure 4-12. If choosing 4 input current sources to pump the current at node V_{x8}, V_{x12}, V_{x14} and V_{x15} and the digital signal input d_1~d_4 as control the switch, the expression of I_{D1} according to the analysis above is given as:

$$I_{D1} = \left[d_1 \frac{1}{2} + d_2 \frac{1}{4} + d_3 \frac{1}{8} + d_4 \frac{1}{16} \right] \cdot I_X \,. \qquad (4\text{-}27)$$

4.6.2 Dummy Transistor String

When the switches shown in Figure 4-12 change their statuses, the current level in the whole transistor string will be changed instantaneously. More important, the node voltage of the output node of the current source which being switched in or out will change significantly. Unless use real large device for the transistor and the switch to realize a small time constant, the glitch due to the changing of current level will experience a long settling time and this excess settling process is the major limitation factor of this current divider DAC being used in high speed applications. In order to solve this problem, either the settling time or the glitch itself has to be improved. As mentioned, the small settling time will unavoidably involve large size transistors and this requirement conflict with the advantage of this current divider DAC with its small area implementation. The solution left is to remove or at least reduce the glitch. By adding a dummy transistor string, the switch will introduce the current to either the main string or the dummy string and the voltage at the output node of all the current sources will only change very slightly if the dummy string is exactly identical with the main string. This structure is shown in Figure 4-13.

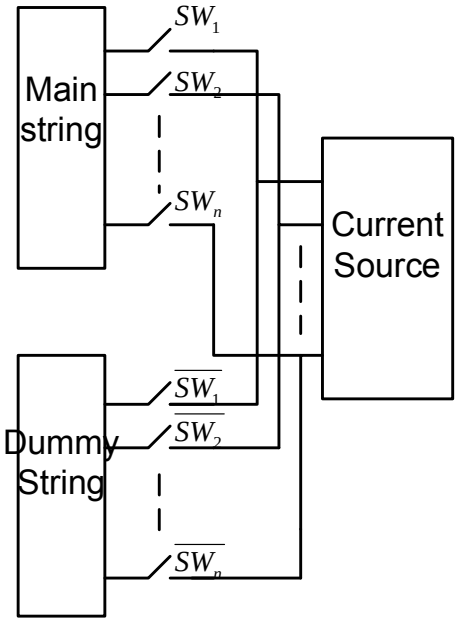
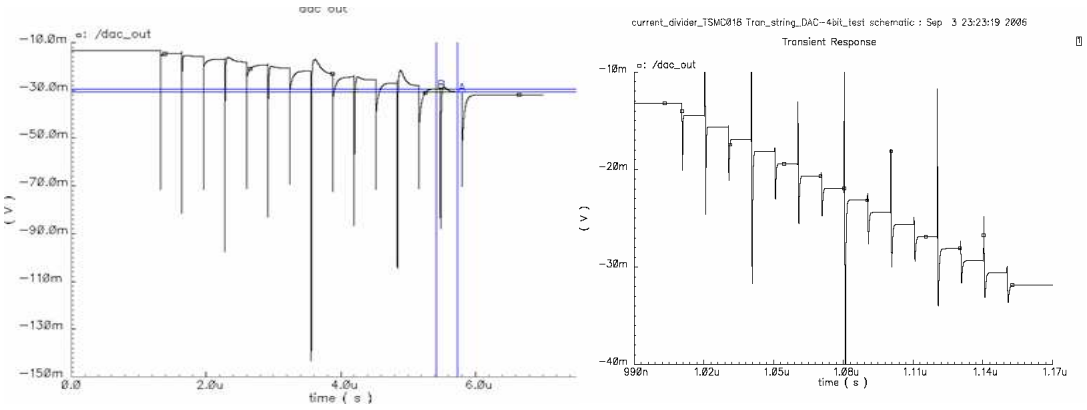


Figure 4- 13 -- Current Division DAC with Dummy String Block Diagram.

The dummy string will significantly reduce the change of current source output voltage and therefore improve the operating speed by orders with the same reference current level.

The simulation of two difference settling procedure is shown in Figure 4-14.



Without Dummy String
(update @ 3 MHz)

With Dummy String
(update @ 100 MHz)

Figure 4- 14 -- Improved Settling Performance with Dummy String.

From Figure 2-14, it is shown that the original structure with no dummy string experienced long settling time and it is not doable for operating only at 3 MHz. After the

dummy string being added, even with 100 MHz update rate, the DAC settles pretty fast since the output nodes of the current sources now has very slightly change in their magnitudes. If the current out of string will not drive the low resistive load directly, the current passing through the string is quite small so that the transistor size is quite limited. The cost of adding a dummy string can almost be neglected but the effect of improving the speed is very significant.

4.6.3 Segment Structure

The most attractive benefit of the current division DAC is its small active area and low power consumption. In order to further reduce the total active area and save more power, a segment structure is developed. The output is binary weighted current and it can be added together directly. The total N bit can be divided as K segment and each segment contains a sub-DAC with the same current division circuit of N/K bits. Within each segment, an N/K bit current divider is placed. The sizing issue now is discussed. For a single transistor string, in order to keep all the transistors working properly, each transistor has to be size for allowable to pass the largest possible current. For the segment structure, for example, if a 6-bit DAC comprises of 3 sub-DACs with each contributing 2 bits as shown in Fig. 15, only the MSB segment need to be sized for the largest current and other transistor size can be scale down by a factor of 4. This scaling down factor will provide higher area efficient to put the MSB with larger silicon area, in which better matching performance is required. Also the current sources can be scaled by the same factor of the transistor strings and the MSB current sources will have the largest the device size and thus share the best matching property. By using segment structure, the area will be further scaled down on the base of current division DAC.

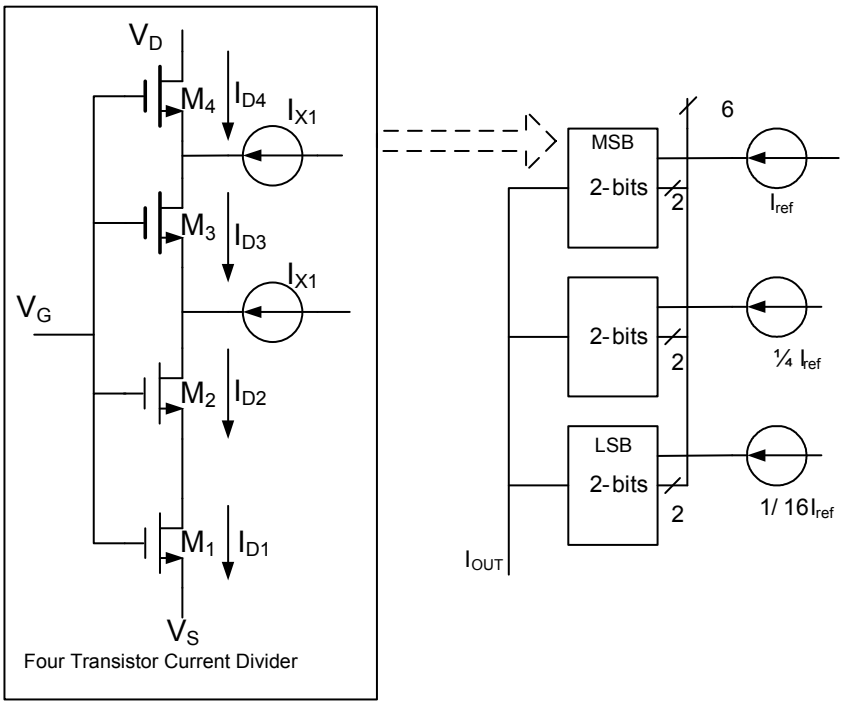


Figure 4- 15-- Segment 6-bit Current Division DAC.

4.6.4 Circuit Building Blocks Implementation

The current sources adopt the well established the wide output range cascode current sources [57]. The reason for cascode is with the concern that the non-ideal current source will introduce moderate nonlinearity into the current divider as we discussed in the previous section. With the scaling down voltage supply, the output swing of the cascode current mirror will waste one more threshold voltage, which is fairly significant in today low voltage supply. The simulation shows that the wide output range cascode current mirror works very well, shown in Figure 4-16.

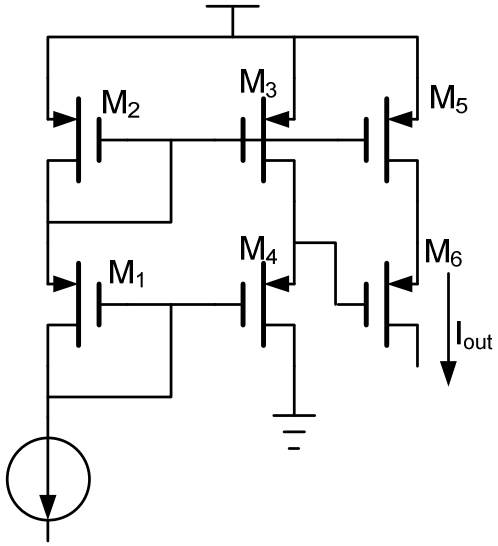


Figure 4- 16 -- Wide Output Range Cascode Current Mirror.

The output stage for the prototype DAC design includes two kinds of structure. The first one is using the op amp to provide the null port. Because this paper will focus on the current division linearity study, the op amp design will not be address in detail here. However, the current division DAC substantially relaxed the offset requirement in the amplifier design compared to other work using deep triode region transistors as resisters [2], in which special circuit was designed for achieving low offset amplifier. In the later part, simulation with different kinds of offset voltages are added to the circuit and this current division DAC has proved to be robust to considerably large offsets.

In the application of the bioelectronics implant systems like in [47]-[49], the DAC needs to drive the resistive load directly at the 1-2 Kilo Ohm level, which is approximately the resistive of human nerve cells. The cascode current mirror is added at the output node. The cascode current mirror will amplify the output current from 10's uA level to several 2 mA level to achieve 2 V p-p signal swing with 1 K ohm load. The cascode current mirror is carefully design with the total number of stage and the size of each stage of NMOS pair and

PMOS pair so that the total overall bandwidth can be optimized. This problem has been addressed in another paper [58]. Compared with the previous published works, [59], the bandwidth of the cascode current mirror can be improved by about 20% according to this new technique.

Another benefit is that this structure offers the options of single and fully differential output almost for free because the dummy string provides the exactly opposite current to the main string. With the differential output, the odd harmonic will be suppressed and the signal will be doubled so that better dynamic range can be obtained with no other extra hardware cost.

4.6.5 Layout and Simulation Results

The 6-bit total active area is about 50um x 50um and the 8-bit current division DAC is about 100um x 100um in TSMC 0.18 um standard CMOS process even with a very loose layout of the digital circuit, which generates the non-overlapping clock for switching the current into either main string or the dummy string. The layout is shown in Figure 4-17.

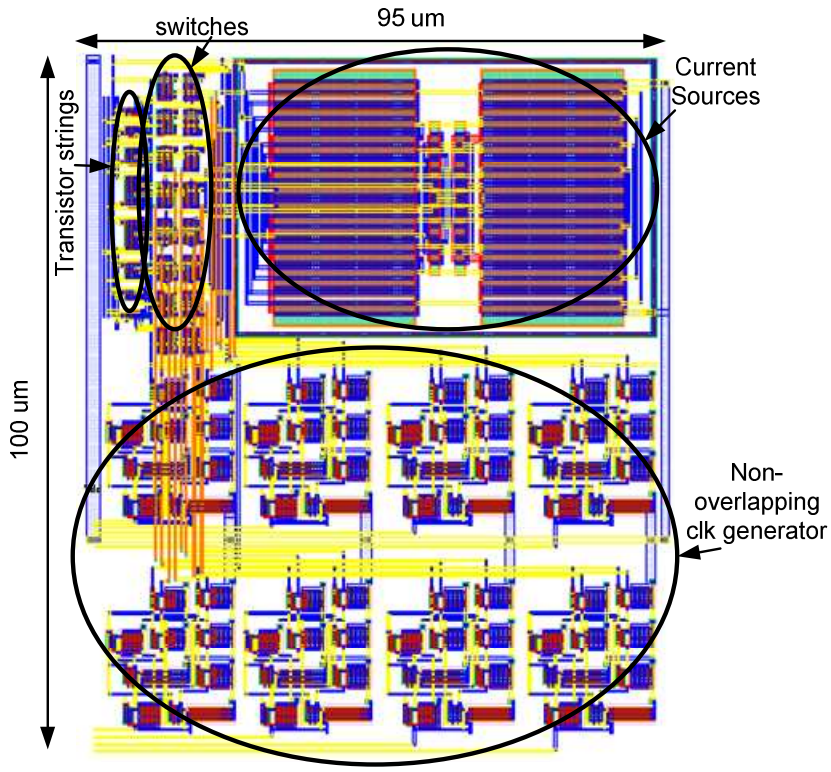


Figure 4- 17 -- 8-bit Current Division DAC Layout

It is obvious that the about 50% are non-overlapping clock generator and this part can be significantly reduced by good digital layout tool and therefore the total active area will be a little more than 60um x 100 um.

In the simulation, two different offset voltages have been added for testify the robustness of the linearity with the changing of the terminal voltages in the current division circuits. The first offset voltage, 50 mV, is added at node V_D in Figure 4-13, which is considerably large and the moderate design efforts should achieve the offset voltage much less than this value. The second offset has been added at the node V_{s_dummy} in Figure 4-13 with the magnitude of 50 mV. The 6-bit DAC is simulated with the cascode current mirror at the output to drive 1 K ohm and 50 ohm load and the results are tabulated in the Table 4-2.

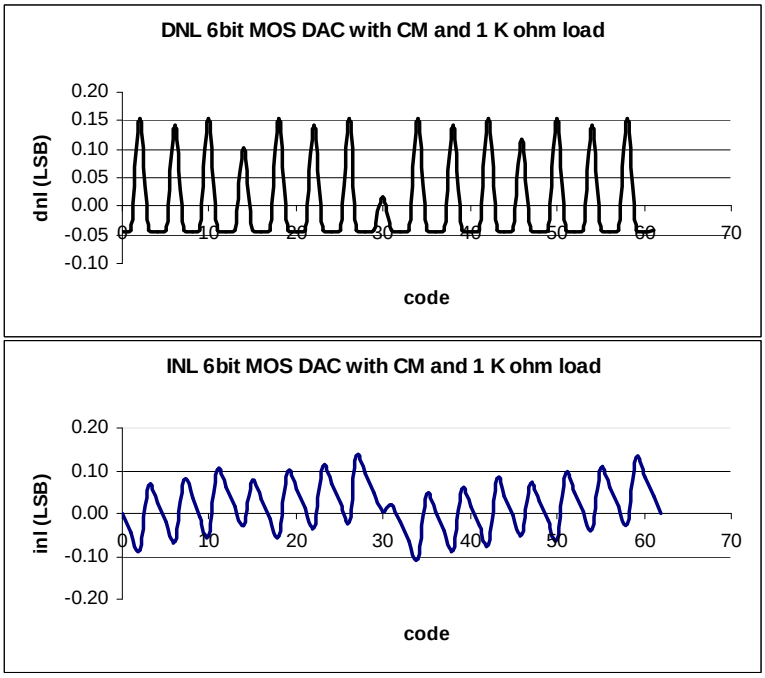


Figure 4- 18 -- Linearity of 6-bif Current Division DAC.

Table 4- 2 Simulation Summary of 6-bit Current Division DAC

6 bit MOS string DAC performance with 1 K/50 ohm load				
static	INL (LSB)		DNL (LSB)	
Load	1 K ohm	50 ohm	1 K ohm	50 ohm
No offest	0.13	0.5	0.15	0.4
Offest 1	0.21	0.7	0.22	0.67
Offestt 2	0.18	0.6	0.2	0.7

From table 4-2, it is easily to observe that this 6-bit current division DAC is robust with the node voltage offsets. With 50 mV offset, appearing at either node V_D or V_{s_dummy}, the linearity only has been deteriorated by very slightly amount. Although the linearity is worse when driving 50 ohm resistor with a much larger current gain current mirror, all the linearity degradation is due to the larger size of the current mirror device. The reference current is 10 uA and the total power consumptions are 2 mW and 36 mW for 1 K ohm load and 50 ohm load, respectively.

For 8-bit DAC design, in order to verify the linearity of the current flowing out of the DAC, this DAC is simulated with a macro model op amp. For achieving 1 V p-p signal with single 1.8 V power supply, a 12.5 K feedback resistor is placed with the op amp and the 80 uA reference current sources is needed. The total power exclude the op amp is 382 uW. The static linearity performance is shown in figure 4-19 and the single and differential ended performance is summered in Table 4-3.

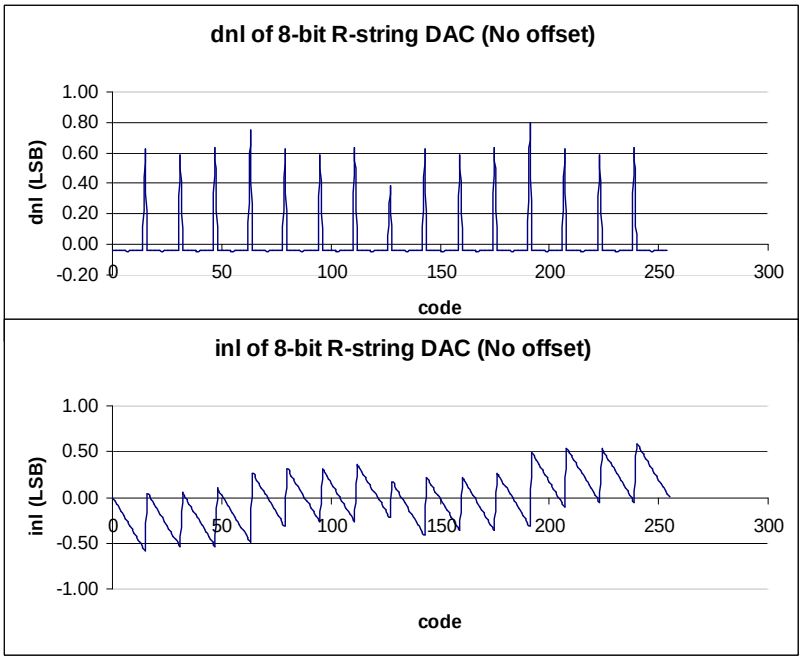


Figure 4- 19 -- Linearity of 8-bit Current Division DAC

Table 4- 3 Single and Differential End 8-bit DAC Linearity

8 bit MOS string DAC performance				
static	INL (LSB)		DNL (LSB)	
single/diff.	Single	Diff.	Single	Diff
No offset	0.5	0.5	0.8	0.8
Offset 1	0.8	0.6	0.65	0.65
Offset 2	0.8	0.6	0.7	0.69

The Dynamic linearity performance is described with spectrum analysis with input frequency keeping increasing close to the Nyquist rate. The single ended and fully differential circuit simulated results are shown in the Figure 4-20 and Figure 4-21, respectively.

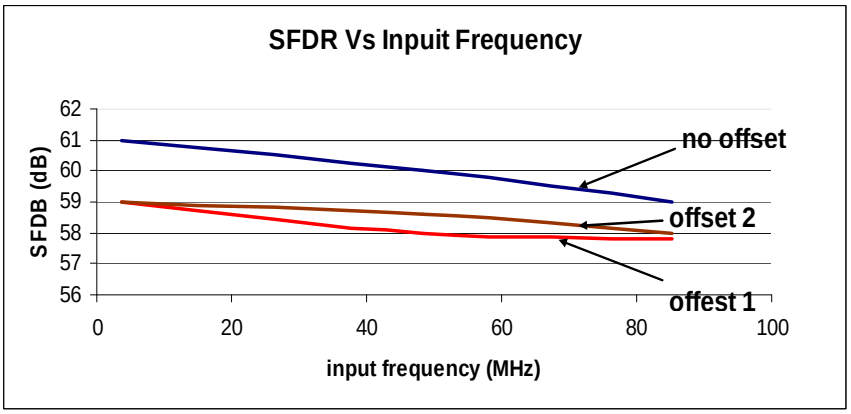


Figure 4- 20 -- SFDR Vs Input Sinu Frequency with Single Ended Circuit.

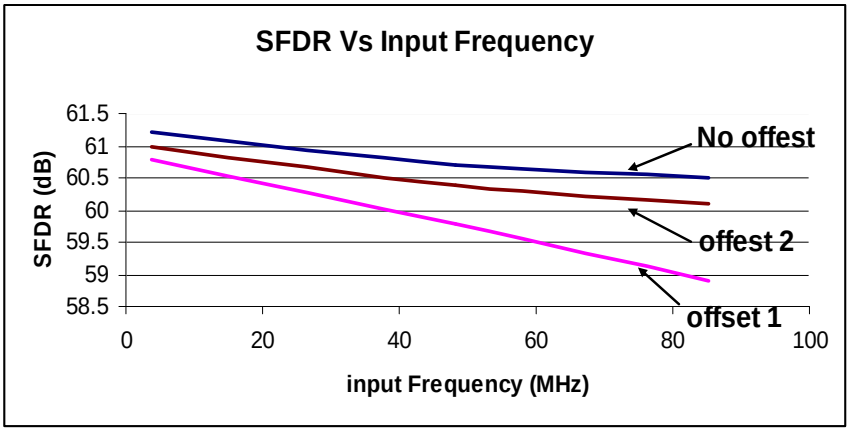


Figure 4- 21 -- SFDR Vs Input Sinu Frequency with Differential Ended Circuit.

From Table 4-3, it is clearly shown that fully differential circuit exhibits better linearity in terms of INL performance because the even harmonics appearing in the slow varying input frequency signal has been suppressed by the differential output. However it won't help with the DNL error caused by non-uniformly spaced step size. This is consistent with noticing in Figure 4-20 and Figure 4-21 that the fully differential circuit provides better

SFDR performance in both cases that offset voltages appears in the circuit. For single ended DAC, if the V_D and V_s share exactly the same voltage, the highest harmonic distortion is 5^{th} harmonic, however, if any offset voltage existing at either V_D node or V_{s_dummy} node, the second harmonic will rise up and determine SFDR. This is why the SFDR of two offset curves is 2 dB lower than the ideal case even without any frequency increase. On the other hand, in the fully differential circuit, even with the offset voltage applied at those two nodes, the even harmonic distortions are still suppressed by the differential output, so that in Figure 4-21, the SFDR with two offsets are very close to the ideal case. Also it shows that this structure is more vulnerable with the offset appearing at the V_D node than at V_{s_dummy} node since in both cases, the "offset 1" curve exhibits better linearity than "offset 2" curves. Beside the minor difference of single end and differential structures, this current divider DAC offers very good linearity within the whole frequency range since the SFDR only drop 2 dB when the input frequency approaching to the Nyquist rate and this also implies that this structure has great potential to operate at higher frequency. The table 4-4 contains the summary of all the major specifications of this 8 bit DAC in differential mode.

Table 4- 4 Summary of the Post-Layout Simulation of 8-bit Current Division DAC

Supply Voltage	1.8 V
Resolution	8 bit
Conversion Rate	200 MHz
INL	0.5 LSB
DNL	0.8 LSB
Settling Time (full ragne to 0.25 LSB, up)	0.78 ns
Settling Time (full ragne to 0.25 LSB, down)	0.88 ns
SFDR @ Nyquist Rate	60.5 dB
Power Consumption (without op amp drive)	382 uW
Die Area	0.01 mm2
Technology	TSMC018

Because it is not very easy to compare the die area for different application DAC with different kinds of load, there is just one comparison listed here for the similar application and the very close current level and technology. Compared with [56], this work offers two times faster operating rate and occupies only roughly 1% of the total active area (normalized to the same feature size). Also the power consumption level and the settling time of this work are compared with several commercial products, which don't drive low resistors directly.

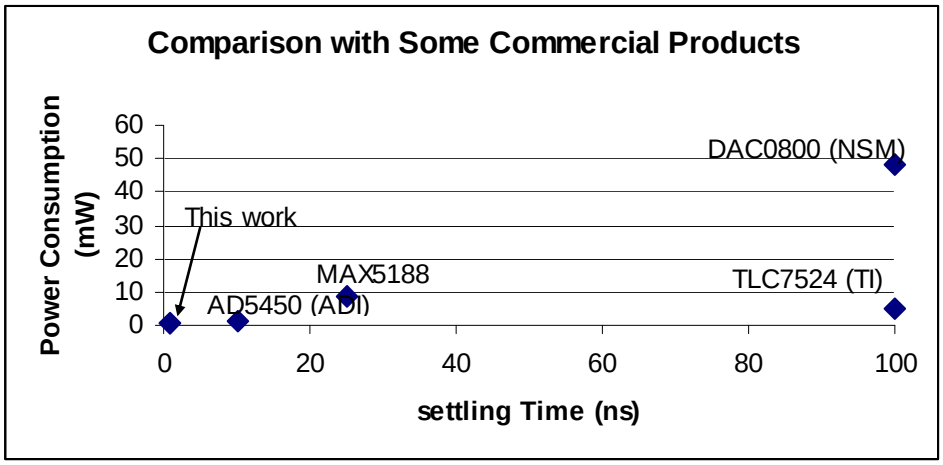


Figure 4- 22 -- Comparison This Work with Some Commercial Products

4.7 Conclusion

This paper presents the study of a well-established technique, which have been influential to many published work in various systems. From the analytical and simulated results, it has been shown that the inherent linearity which has been claimed by the original authors is actually quite limited and also dependent on multiple circuit conditions. The phenomenal linear performance reported by all the works based on this current division circuit are actually based on more general circuit principle; symmetrical property. In the second part of this paper, a novel current division DAC has been presented. For low resolution design, this

current divider DAC benefit from that current division circuit with very small active area and low power consumption. Also its straightforward circuit and immunity with large offset voltage simplify the design efforts. The dummy string dramatically boosts the operating speed with very slight cost of the extra silicon area. Also this DAC provides fully differential output with no extra hardware and thus offers better static and dynamic linearity and dynamic range. The simulations demonstrate potent for higher speed operating with excellent settling performance.

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CHAPTER 5 BANDWIDTH OPTIMIZATION OF CMOS CURRENT MIRRORS

5.1 Introduction

Current mirror is one of the most useful basic building blocks in CMOS integrated circuit. The performance of current mirrors usually determines the whole circuit performance, especially in some current conveyors and other current mode circuits. The comparison of difference current mirror structures such as simple current mirror, Wilson current mirror, cascode current mirror, etc have been report in [1]. The several major specifications have been compared in this work including output resistance, bandwidth and current gain. However, beside [2], very few reported works address the issue about optimization design with a chosen structure. This work will present the approach of optimization of a cascade simple current mirror with a given current gain. The analysis and simulation exhibit that by choosing proper number of stage and carefully allocating the gain of each stage, the bandwidth of the total current mirror would be maximized. This work would be particular interested for those circuits needs to drive large capacitance load or low resistance load with cascade current mirror, such as dressed in [3], [4].

5.2 Simple Cascaded CMOS Current Mirrors Analysis

The bandwidth optimization problem has been already addressed in [2]. However, the previous work based its conclusion mainly upon simulation and, even though the equations have been presented, the best choice of number of stage and gain arrangement for each stage has not been clearly addressed. Furthermore, the bandwidth of the current mirror still can be

improved with more delicate analysis. In the following part, a close form expression of the bandwidth will be derived based on single pole system approximation.

The single stage current mirror is shown below in Figure 5-1. When the large current gain is required, a very wide transistor is necessary for the output device and thus large parasitic capacitor associating with C_{gs} will limit the bandwidth of this current mirror. The total capacitance approximately equals to the sum of the two C_{gs} and the total equivalent resistance roughly equals to the $1/g_{m1}$. The size of M_2 has been uniquely defined by the total current gain and the design space contains only one design parameter $\{W_2\}$, assuming the identical length has been used for good matching performance.

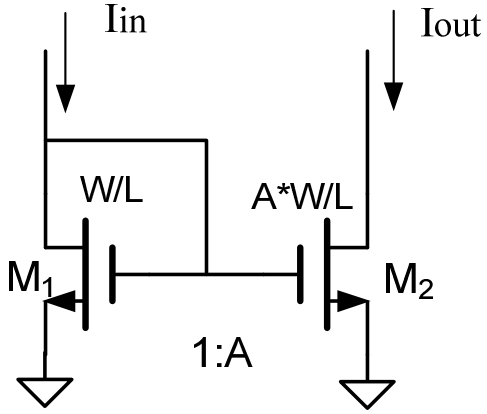

Figure 5- 1 -- Simple Current Mirror with Current Gain of A

$$C_{gs1} = \frac{2}{3} C_{OX} W_1 L_1, \tag{5- 1}$$

$$C_{gs2} = \frac{2}{3} C_{OX} W_2 L_2 = \frac{2}{3} A C_{OX} W_1 L_1, \tag{5- 2}$$

$$R_{eq} = \frac{1}{g_{m1}} = \frac{L_1}{\mu_n C_{OX} W_1 V_{eb}}, \tag{5- 3}$$

$$\tau_{eq} = R_{eq} \cdot C_{tot} = R_{eq} \cdot \left(C_{gs1} + C_{gs2}\right) = \frac{2}{3} \frac{L_1^2}{\mu_n V_{eb}} (1 + A). \tag{5- 4}$$

Alternatively, by replacing the single large transistor in Figure 5-1 by multiple stages of current mirrors, the bandwidth of the current mirror could be significantly increased and meanwhile the total current gain is still maintained. For cascade current mirror, two different scenarios will be discussed in the following part, even number of stages and odd number of stages. First, the bandwidth expression of even number of stage cascade current mirror will be derived below.

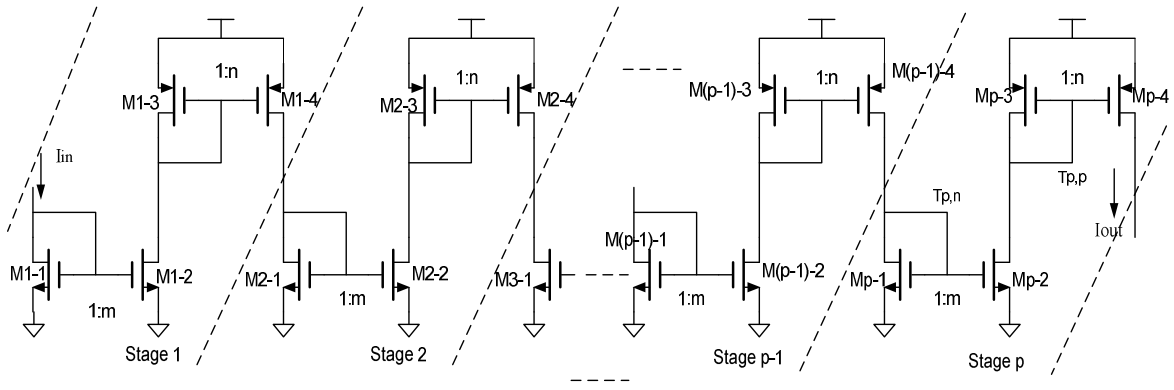

Figure 5- 2 -- a Cascade Current Mirror with Even Number of Stages

For even number of stages, it is convenient to group the NMOS and PMOS pair as a single stage and total number of this P-N MOS pair is nominated as "*P*". Unlike the single stage case, in which only one design parameter is available, there are total 2P design parameters comprising of a 2P dimensional optimization problem, {$W_{1\text{-}2}$, $W_{1\text{-}4}$, $W_{2\text{-}2}$, $W_{2\text{-}4}$, …, $W_{p\text{-}2}$, …, $W_{p\text{-}4}$}. It is pretty hard to result an optimization problem with high order dimensions and thus certain assumption needs to be presented here. Assume the gains of all NMOS pairs are the same as "*m*" and the gain of every PMOS pair is identical, "*n*". If the second order effect has been neglected here and also the overdrive voltage of the NMOS pair and PMOS pair are

assumed to be the same, the geometry ratio of each current mirror stage is defined by the corresponding mirror gain as listed below:

$$\left(\frac{W}{L}\right)_{1-1}=\left(\frac{W}{L}\right)_1, \qquad \left(\frac{W}{L}\right)_{1-2}=\left(\frac{W}{L}\right)_1\cdot m,$$

$$\left(\frac{W}{L}\right)_{1-3}=\left(\frac{W}{L}\right)_1\cdot m\cdot\lambda, \qquad \left(\frac{W}{L}\right)_{1-4}=\left(\frac{W}{L}\right)_1\cdot m\cdot\lambda\cdot n, \quad \ldots,$$

$$\left(\frac{W}{L}\right)_{p-3}=\left(\frac{W}{L}\right)_1\cdot m^p\cdot n^{p-1}\cdot\lambda, \quad \left(\frac{W}{L}\right)_{p-4}=\left(\frac{W}{L}\right)_1\cdot m^p\cdot n^p\cdot\lambda,$$

where $\lambda=\frac{\mu_n}{\mu_p}$.

It is clearly to see that: $(n\cdot m)^p=A$.

Use the similar process as single stage current mirror, the time constant associate with the node at PMOS pair of the p-th stage is expressed as the multiple of the total equivalent capacitance and resistance. The time constant is derived as:

$$\begin{aligned} C_{tot,p-p}&\cong C_{gs,p-3}+C_{gs,p-4}=\frac{2}{3}C_{ox}m^p n^{p-1}W_1L_1\lambda+\frac{2}{3}C_{ox}m^p n^p W_1L_1\lambda \\ &=\frac{2}{3}\lambda C_{ox}W_1L_1A\left(1+\frac{1}{n}\right) \end{aligned} \tag{5- 5}$$

$$R_{tot,p-p}\cong\frac{1}{g_{m,p-3}}=\frac{1}{K_p\left(\frac{W}{L}\right)_{p-3}V_{eb}}=\frac{L_1 n}{K_p\lambda A W_1 V_{eb}}, \tag{5- 6}$$

$$\tau_{p-p}=C_{tot}\cdot R_{tot}=\frac{2}{3}\frac{L_1^2(n+1)}{\mu_p V_{eb}}. \tag{5- 7}$$

Use the same procedure, the time constant associate with the NMOS pair at the p-th stage is given:

$$\tau_{p-n} = C_{tot,p-n} \cdot R_{tot,p-n} = \frac{2}{3}\frac{L_1^2}{\mu_n V_{eb}}\left(1+\frac{A^{1/p}}{n}\right). \quad (5\text{-}8)$$

Repeat this derivation procedure for all the nodes associated with the NMOS and PMOS mirror pair, it is interested to discover that all the NMOS pairs share the same close form expression and so does the PMOS pair. The expressions of the time constant according to the NMOS pair mirrors and PMOS mirror pairs are shown below, respectively.

$$\tau_{i-n} = \frac{2}{3}\frac{L_1^2}{\mu_n V_{eb}}\left(1+\frac{A^{1/p}}{n}\right), \quad (5\text{-}9)$$

$$\tau_{i-p} = \frac{2}{3}\frac{L_1^2(n+1)}{\mu_p V_{eb}}. \quad (5\text{-}10)$$

Based on the assumption:

$$\tau_{tot} \cong \sum \tau_{i-n} + \sum \tau_{i-p}\,. \quad (5\text{-}11)$$

it is easily to derive the expression of the total equivalent time constant as:

$$\begin{aligned}\tau_{tot} &= \sum \tau_n + \sum \tau_p = \frac{2}{3}\frac{L_1^2}{\mu_n V_{eb}}\left(1+\frac{A^{1/p}}{n}\right)\cdot p + \frac{2}{3}\frac{L_1^2(n+1)}{\mu_p V_{eb}}\cdot p \\ &= \frac{2}{3}\frac{L_1^2 p}{V_{eb}}\left[\frac{(1+n)}{\mu_p} + \frac{(1+\frac{A^{1/p}}{n})}{\mu_n}\right]\end{aligned} \quad (5\text{-}12)$$

For achieving the maximum bandwidth, it is equivalently to find the smallest time constant with certain values of *n* and *p* in (5-12). Take the partial derivative of (5-12) versus *n*, it is given:

$$\frac{\partial \tau_{tot}}{\partial n} = \frac{2}{3}\frac{L_1^2 p}{V_{eb}}\left[\frac{1}{\mu_p} + \frac{A^{\frac{1}{p}}}{\mu_n}\left(-\frac{1}{n^2}\right)\right]. \quad (5\text{-}13)$$

By equating (2-13) to zero, the value of *n* is given:

$$n = \sqrt{\frac{\mu_p}{\mu_n}} A^{\frac{1}{2p}}. \qquad (5\text{- }14)$$

Eq. (5-14) gives the specific value for each given p to achieve the optimum bandwidth of certain current gain.

In the following section, the cascade current mirror with odd number of stage will be studied. As shown in Figure 5-3, the odd number of stage can be also treated as integer number of PMOS-NMOS pair plus one more NMOS current mirror.

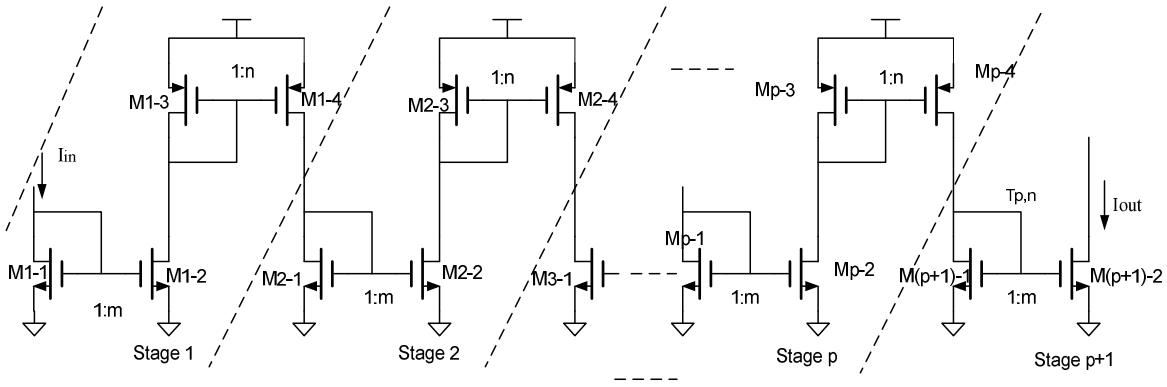

Figure 5- 3 -- a Cascade Current Mirror with Odd Number of Stages

The analysis is almost the same as previous section for even number of stages except the relationship between the NMOS pair gain, PMOS gain and total current gain is now given:

$$m^{p+1} \cdot n^p = A. \qquad (5\text{- }15)$$

With the same analytical procedure, the time constant associate with NMOS and PMOS mirror pairs are given as:

$$\tau_{i-n} = \frac{2}{3}\frac{L_1^2}{\mu_n V_{eb}}\left(1 + \frac{A^{1/(p+1)}}{n^{p/(p+1)}}\right), \qquad (5\text{- }16)$$

$$\tau_{i-p} = \frac{2}{3}\frac{L_1^2(n+1)}{\mu_p V_{eb}}. \tag{5- 17}$$

The total equivalent time constant is:

$$\begin{aligned}\tau_{tot} &= \tau_{i-n}\cdot(p+1)+\tau_{i-p}\cdot(p)\\ &= \frac{2}{3}\frac{L_1^2}{V_{eb}}\left[\frac{(1+n)\cdot p}{\mu_p}+\frac{(p+1)\cdot\left(1+\frac{A^{1/(p+1)}}{n^{p/(p+1)}}\right)}{\mu_n}\right].\end{aligned} \tag{5- 18}$$

To find the proper value n to achieve optimum bandwidth, take the partial derivative to (5-18) and solve for n:

$$n = \left[\frac{\mu_p}{\mu_n}A^{\left(1/p+1\right)}\right]^{\left(p+1/2p+1\right)}. \tag{5- 19}$$

The optimum bandwidth of the cascade current mirrors can be realize by properly chosen the PMOS gain according to the equation (5-14) and (5-19) for even order cascade stage and odd order cascade stages, respectively. The values of the PMOS mirror gain for optimizing the overall bandwidth with total current gain equals to 50, 300, 1000 are tabulated in Table 5-1 for different number of stages.

Table 5- 1 Optimum Gain Allocation for PMOS Mirror Pair

Overall Current Gain A			
p (# of stages)	50	300	1000
2	3.2	7.8	14.3
3	1.3	2.3	3.45
4	1.2	1.9	2.53
5	0.8	1.2	1.53
6	0.9	1.2	1.42
7	0.7	0.9	1.08
8	0.7	0.9	1.07

This analysis results a close form expression of the bandwidth of cascade current mirror and furthermore exhibits a fairly simple method to design a cascade current mirror with a maximized bandwidth: the optimum bandwidth can be obtained by using (5-12) and (5-18) with corresponding values of *n* from (5-14) and (5-19) for integer number of stage *p*. The bandwidths of multiple stage current mirrors are shown in Table 5-2 below.

Table 5- 2 Optimum Bandwidth for Multiple Cascade Current Mirrors

Overall Current Gain A			
p (# of stages)	**50**	**300**	**1000**
1	2.71E+07	4.59E+06	1.38E+06
2	3.70E+07	1.67E+07	9.44E+06
3	**5.37E+07**	**3.36E+07**	2.38E+07
4	3.90E+07	2.83E+07	2.24E+07
5	4.12E+07	3.25E+07	**2.74E+07**
6	3.19E+07	2.65E+07	2.31E+07
7	3.21E+07	2.76E+07	2.47E+07
8	2.62E+07	2.31E+07	2.10E+07

From Table 5-2, it is clearly shown that the largest bandwidth can always be obtained with odd number of stages cascaded and odd number cases exhibits better bandwidth than even order cases except for single stage. For instance, 3-stage cascade is the fastest one for overall current gain of 50 and 300 and the 5-stage structure has the largest bandwidth for current gain of 1000. This saw shape bandwidth curve is mainly due to the output stage device type. For the structure shown in Figure 5-2 and Figure 5-3, the input mirror pairs are N-channel transistor and output mirror pairs are also N-channel devices if odd number of stages has been used. N-channel transistor has much smaller size compared to the P-channel device for the same magnitude of the current and therefore the time constant associated with the total

parasitic capacitance will be significantly smaller in N-channel transistors than in P-channel transistors.

In the next section, the simulation will be presented to verify this optimization analysis. Also, the comparison will be show between this work with the previous work and certain common wisdom.

5.3 Simulation and Comparison

In the previous section, the analytical work demonstrates close form expressions for optimum bandwidth of the cascade current mirror. The simulation is necessary to verify the analytical results because the square law model cannot accurate predict the performance of modern semiconductor circuits. The cascade current mirrors have been design using TSMC 0.18 um process with cadence environment. There are total three different overall current gains are chosen for the simulations, 50, 300 and 1000. Figure 5-4, 5-5 and 5-6 show the simulated bandwidth comparing with the analytical bandwidth, respectively

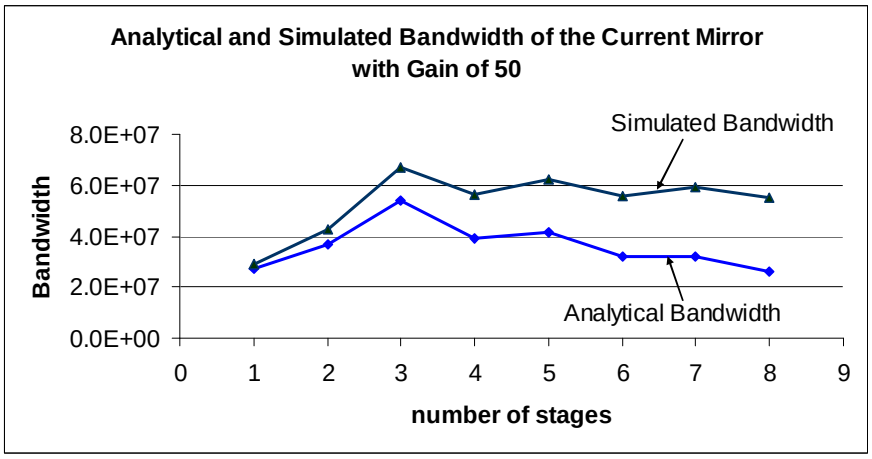

Figure 5- 4 -- Simulated and Analytical Bandwidth with Current Gain of 50.

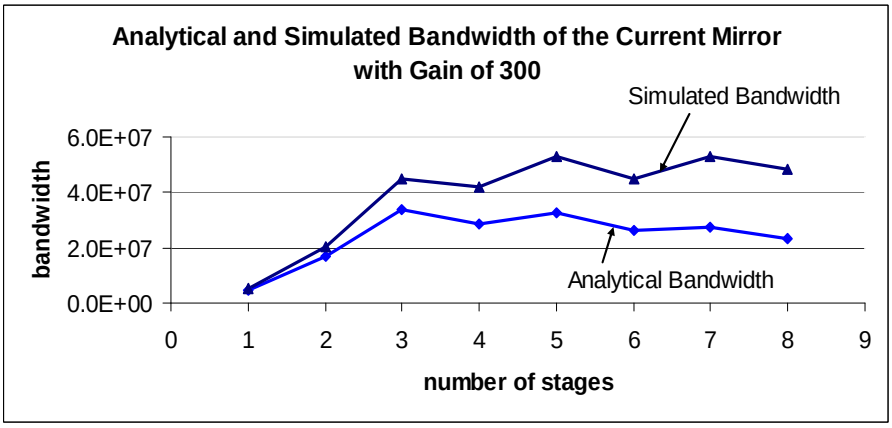

Figure 5- 5 -- Simulated and Analytical Bandwidth with Current Gain of 300.

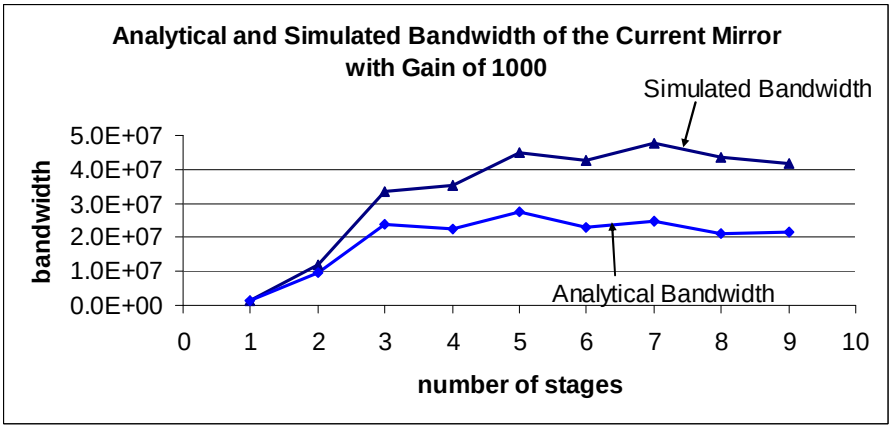

Figure 5- 6 -- Simulated and Analytical Bandwidth with Current Gain of 1000.

From above figures, the match between analytical work and simulation results has been demonstrated, especially for lower number of cascaded-stages. With the increasing number of the stages, the difference between the analytical results and simulations is getting bigger. For example, the 3-stage cascaded current mirror has been proved to be the fastest one in both analytical and simulation works for current gain of 50, however, 7-stage structure exhibits the highest bandwidth from the simulation results of gain of 1000 instead of 5-stage in the analytical work. This is because with the increasing number of stage, the approximation from (5-11) becomes more and more rough and the analytical results diverts

from simulation further. Even though, the difference does exist between the analytical and simulation results, this approach provides a very good starting point when the optimization of a cascaded current mirror is of interested for choosing the proper number of stage and gain allocation for each stage. In the next part, this work will be compared with the previous approach and some common wisdom. In the previous work [2], the author did not clearly address the gain for each stage besides those two equations below, where nn and np represent the number of stage of NMOS mirror and PMOS pair, respectively:

$$f_1(m,n): m^{nn} \cdot n^{np} = A, \tag{5- 20}$$

$$f_2(m,n): \sqrt{m}(1+m)^2 = \frac{\mu_n}{\mu_p}\sqrt{n}(1+n)^2. \tag{5- 21}$$

The Newton iteration can be used to solve above two equations for numerical solutions.

$$\begin{pmatrix} m_{i+1} \\ n_{i+1} \end{pmatrix} = \begin{pmatrix} m_i \\ n_i \end{pmatrix} - \gamma [DF]^{-1} \begin{pmatrix} f_1(m_i, n_i) \\ f_2(m_i, n_i) \end{pmatrix}, \tag{5- 22}$$

where $DF = \partial \begin{pmatrix} f_1 \\ f_2 \end{pmatrix} \Big/ \partial \begin{pmatrix} m \\ n \end{pmatrix}$. (5- 23)

Solving above equations for different number of stages, the optimized the bandwidth current mirror are achieved and then the comparison can be presented between this work and the previous work for the same overall current gain. Also this optimization problem is analogous to the sizing of a string of inverters for driving large capacitive loads. The common wisdom will set the gain of each stage identical and given as:

$$n = \sqrt[p]{A}. \tag{5- 24}$$

The following three figures show the comparisons of this work with previous (Kirk Peterson) work and common wisdom for difference overall current gain and different number of total stages.

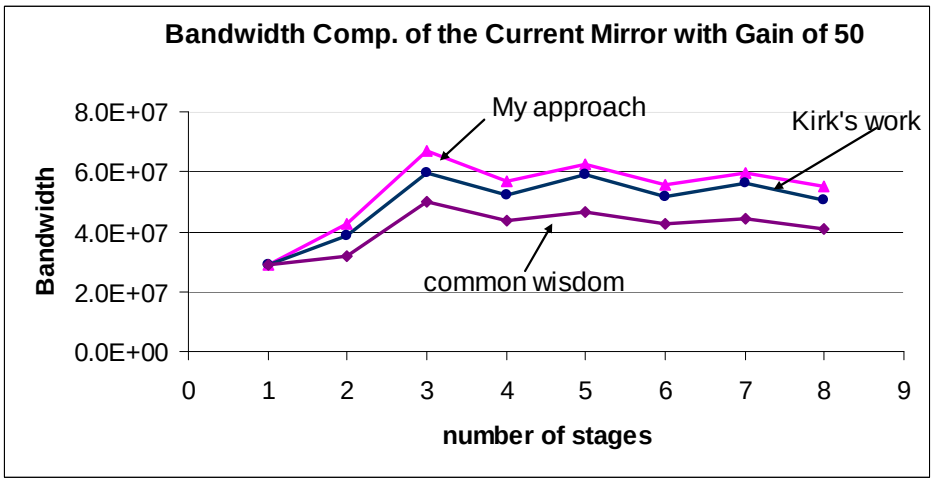

Figure 5- 7 -- Bandwidth Comparison of This work, Previous Work and Common Wisdom-set I.

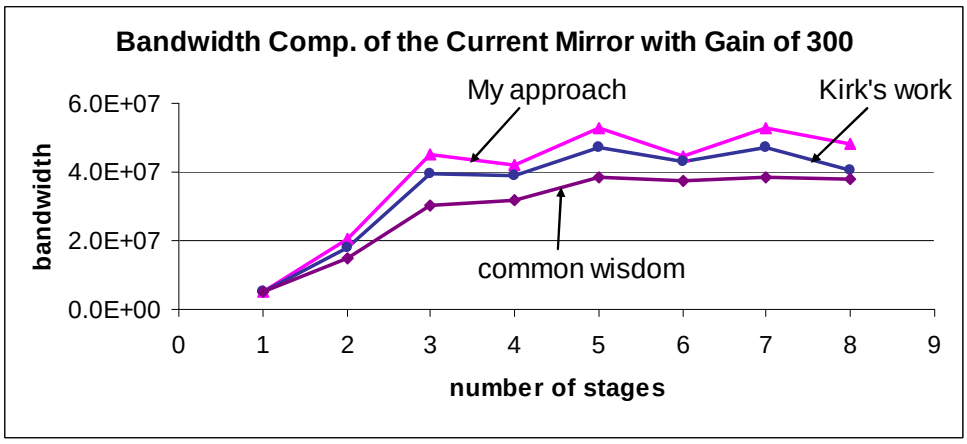

Figure 5- 8 -- Bandwidth Comparison of This work, Previous Work and Common Wisdom –II.

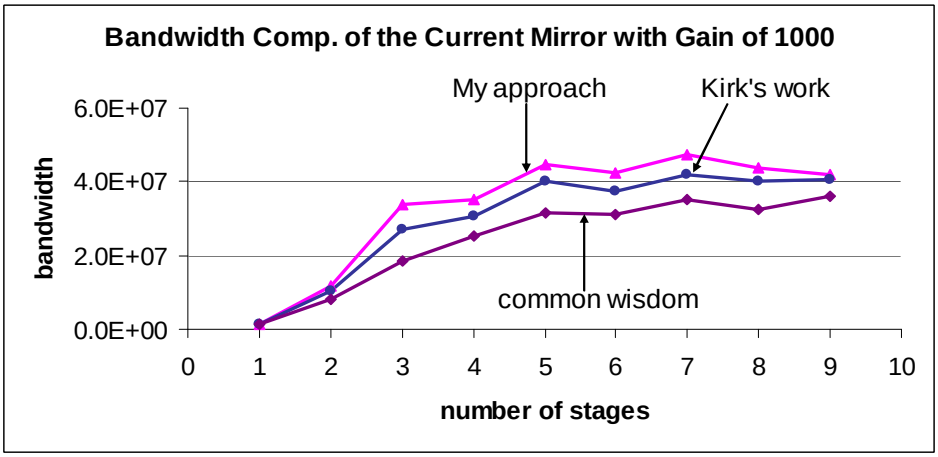

Figure 5- 9 -- Bandwidth Comparison of This work, Previous Work and Common Wisdom –III.

From above three figures, it is clearly shown that this approach has a significant improved best bandwidth than common wisdom and compared to the previous work, this work results about 10% to 25% increased largest bandwidth for different current gains. In order to verify this work, some random gain allocations have been chosen for certain number of stages near the neighborhood of the optimized design. For instance, 4, 5, 7 stages current mirrors have been simulated with some random ranged gain for each stage for gain of 50 and all the results have been shown in the figure below.

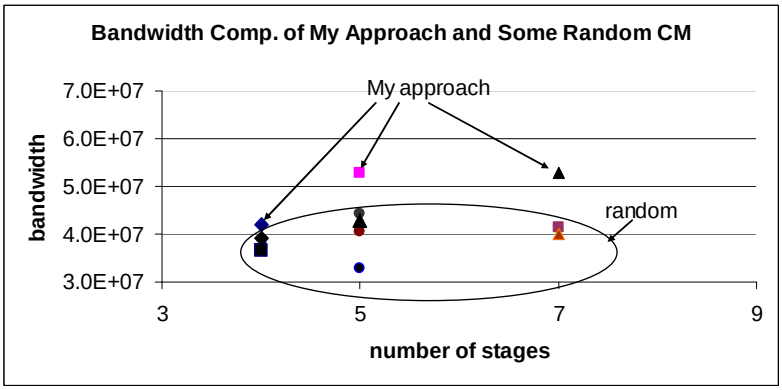

Figure 5- 10 -- Comparison of Bandwidth of This work, with Some Random Gain Arranged Current Mirror with Overall Gain of 50.

It is very obviously that this work exhibits much better bandwidth than all the random chosen mirrors. Combined Figure 5-7~ Figure 5-10, it has been proved that this work will produce the highest bandwidth cascaded current mirror for a given overall current gain among existing design strategies.

5.4 Conclusion

An effective design approach has been presented in this paper and the near-optimum bandwidth of a cascaded current mirror can be achieved by choosing the proper values of number of mirror stages and the specific gain for each stage according to this analytical work. Even thought, the theoretical results have some difference from the simulation results, this work still provides a very good guidance and starting point for designing the cascaded current mirror when the bandwidth is important. From all the simulation results it has been shown that this work produced higher bandwidth than the previous work and some random gain allocations structures.

5.5 References

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CHAPTER 6 A COMPREHENSIVE STUDY OF CALIBRATION ALGORITHMS FOR PIPELINE ADCS

Abstract--various calibration algorithms were introduced in the literature to improve the linearity performance of pipeline analog-to-digital converter (ADC). In the first part of this chapter, a comparison study of the reported calibration algorithms will be presented, including the basic analysis on the purpose of ADC calibration algorithms, the discussion and comparison of the representative reported algorithms. The insight characteristics of those algorithms are investigated and the advantages and possible limitations are addressed for each algorithm according to the implementation cost and performance improvement. In the second part of this chapter, an original model based calibration algorithm is carried out with more details in theoretical analysis and simulation results. Based on the examination of both existing and proposed algorithms, the comprehensive review of the existing algorithms and the prediction of the next generation calibration algorithm to improve the pipeline ADC linearity beyond 14 bit level will be included as the conclusion for this chapter.

6.1 Introduction

Data converter is well known as the world largest volume mix-signal component and is wildly used in communication, signal processing and electron medical systems. The pipeline ADC is one of the most popular and widely used architecture among the Nyquist rate ADC architectures due to its high resolution with modest high speed. However, the shrinking design feature size and decreasing supply voltage make the design work more and more difficult with more ambitious target. Meanwhile there are many issues that limit the

overall performance such as finite and nonlinear operational amplifier (op-amp) gain, mismatch and voltage dependent capacitance of capacitors in switch capacitor circuits, comparator offset error and so on. To achieve high performance under these conditions, calibration algorithms were introduced into ADC design work since 1980's. Although there are many calibration algorithms reported in past twenty years, the experimental performance of most reported calibration algorithms has not been impressive and there has been minimal industrial adoption of these techniques. Table 6-1 will give the summary of the most popular and more recent results on ADC calibration that have appeared in the literature. These reported works including different calibration method, analog and digital, achieves different ADC performance with, of course, different hardware or software costs.

Table 6- 1 Comparison of Recent Calibration Performance of Pipeline ADCs

Year	Author	Resolution (bits)	Speed (MSPS)	INL (LSB)	ENOB	Calibration
1991	Lin, Kim and Gray	13	2.5	2	11	capacitor-triming, on-chip
1993	Karanicolas, A.N	15	1	1.25	13.678	Digiral, off-chip
1995	Kwak, Song	13	10	1.8	11.152	Digital, off-chip
1996	Mayes, M.K	16	1	0.75	15.415	Digital, on-chip
1997	Song, B.S	15	5	1.77	13.176	Digital, background
1998	Wooley, B.A	12	10	0.9	11.152	Analog, off-chip
1998	Lewis, S.H	10	40	0.84	9.251	Digiral, on-chip
1999	Erdogan, O.E	12	0.125	0.71	11.494	Digital, on-chip
2000	Blecker, E.B	8	13	0.6	7.737	Digital, background
2000	Opris,I.E	14	5	1.5	12.415	self-calibration
2002	Chuang, Y.H	14	10	2.5	11.678	Digital, on-chip
2002	Lewis, S.H	10	120	0.88	9.184	Digital, background
2002	Shabra, A	12	61	0.6	11.737	self-calibration
2003	Beck and Allstot	8	20	0.65	7.621	No
2004	Lewis	12	80	0.24	12	Digital calibration

From Table 6-1, it is clearly shown that all the authors achieved performance improvement with the introduced calibration algorithms and some claimed the resolution after calibration at reasonably high levels. However, the effective resolution based upon INL performance for low-frequency inputs of the higher-speed structures, specifically, the 10 MHz and beyond structures, are limited to the 12-bit level. The results, including some of the lower-speed structures, are compared graphically in the following Figure 6-1.

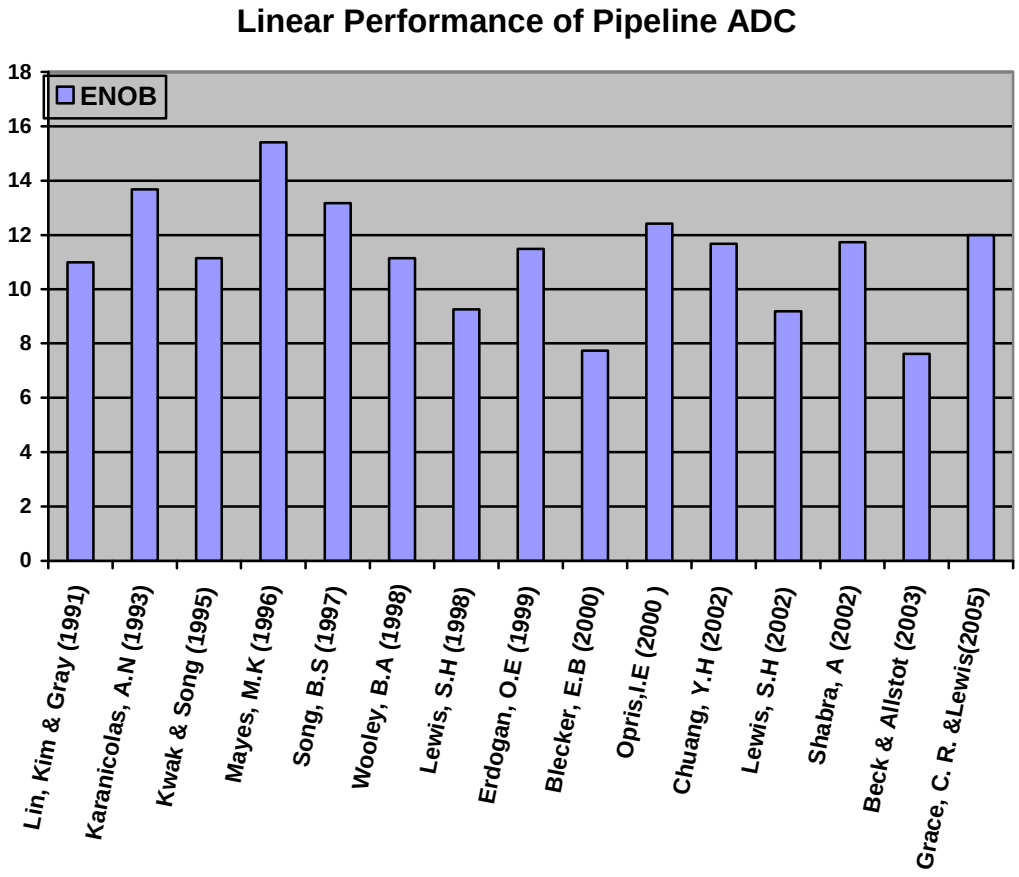


Figure 6- 1 -- Linearity Performance Comparison of Selected Pipeline ADCs with Calibration

6.2 Comparison of the Existing Calibration Algorithms

Existing calibration algorithms can be classified into one of two types. One is digital calibration algorithms in which the raw digital output codes are corrected with some form of digital signal processing and the other is analog calibration (alternatively termed hardware calibration) in which analog circuitry is calibrated so that ideally the natural digital output code is correct. Some authors use the term "software calibration" interchangeably with the term "digital calibration". Most of the digital correction algorithms require insertion of a test or training signal into the signal path or to intermediate points in the signal path to excite and hence correct the non-idealities of the ADC. Some analog calibration algorithms also require test or training signals. Any digital or analog calibration algorithm can be classified into one of two types. One focuses on correcting the source of the errors and the other focuses on correcting the effects of the non-idealities in the signal path. Both background and foreground variants of analog and digital calibration algorithms have been reported in the literature. Collectively, all reported analog and digital calibration algorithms share two properties. First, they are strongly dependent upon the model of the constituent blocks of the ADC and second, they focus on calibration of some intermediate characteristics of the ADC. As a consequence, most are highly sensitive to the accuracy of the models and even modest model errors seriously limit the performance of these algorithms. Since the calibration focuses on adjusting or trimming some intermediate parameter such as a gain error in an inter-stage amplifier or a discontinuity in the transfer characteristics of the ADC, there is no assurance that calibrating these intermediate parameters will result in achieving good desired performance parameters.

6.2.1 Introduction of Pipeline ADC and Purpose of Calibrations

A brief analysis of the ADC and ADC calibration is introduced here as the base of the following evaluation.

At low frequencies, an ADC can be characterized by an ordered sequence of voltage or current transition points which divide the input range of the ADC into a sequence of intervals where the transition points in the sequence are rank ordered by the value of the voltage or current. The intervals, in turn, are mapped into an ordered sequence of digital numbers with the position of any interval in the interval sequence being determined by the position of the two transition points that define the interval in the transition point sequence.

For an ideal ADC, the number of and location of the transition points is determined by the ADC architecture and the transition points should be uniformly distributed throughout the input range of the ADC. The interval sequence is mapped into the non-negative integers defined by the position of the interval in the sequence with the first position in the sequence being mapped to the integer 0. The integers are generally expressed in the base-2 number system and generally referred to as digital numbers or digital codes.

A fabricated ADC will have errors in the location of the transition points, some transition points may be missing, and there may be errors in the digital code mapping of the intervals. After fabrication, calibration can be used to reduce the errors. This calibration is generally performed on-chip and termed self-calibration. The static performance metrics, INL and DNL, are widely used to characterize the low-frequency performance of the ADC. Both are defined in terms of the transition points of the ADC and are measures of how uniformly the transition points are spaced. Invariably, calibration algorithms are developed for the purpose of improving the INL and DNL metrics of a device.

Non-idealities in an ADC are all due to non-ideal performance of the circuit used to implement the ADC and thus can be classified as hardware errors. As to the pipeline architecture, the non-idealities can be classified into two types. One is the linear error and the other is the nonlinear error. A Pipeline ADC is composed of multiple pipeline stages. There are many sources of errors in a pipeline stage, such as the inter-stage transfer gain error and reference voltage errors. Some of the errors such as the reference errors can be viewed as linear errors, which will results some sorts of linear shift range of the final outputs, and the others such as the nonlinear transfer gain error can be viewed as nonlinear errors, which will leads to nonlinear shape of transfer curve instead of the ideal linear relationship between the analog input and digital outputs.

In order to work through the calibration algorithms that focus on the different error sources causing the nonlinearity, in this section, we will review the pipelined architecture briefly and analyze its possible errors. A pipeline ADC is composed of some pipeline stages. Each pipeline stage receives the analog signal from the previous stage (or the original input for the 1st stage), and outputs one or multiple digits and a residue voltage to the next stage. The most simple and widely used pipelined architecture is the one bit per stage architecture this architecture will be our example to propose this new calibration scheme due to its simplicity and popularity. A typical 1-bit pipeline structure is shown in Figure 6-2.

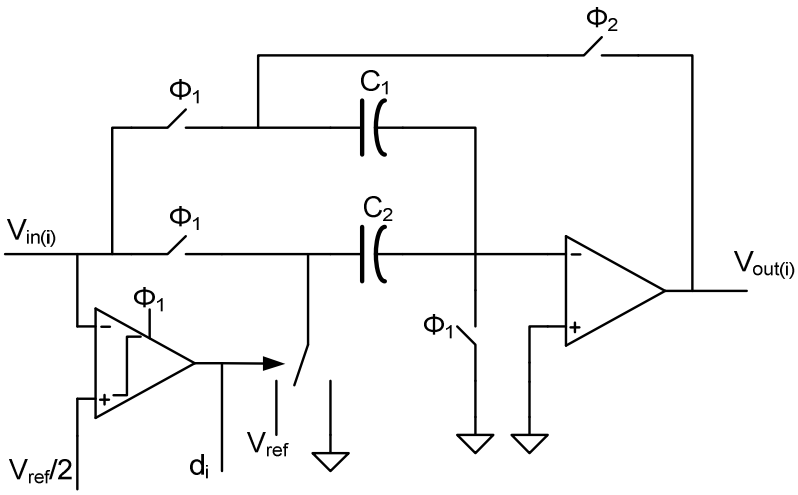


Figure 6- 2 -- One bit/stage pipeline stage structure at Stage-i

For the structure shown in Figure 6-2, the input range is [0, V_{ref}]. The comparator threshold voltage is $V_{th}=V_{ref}/2$. When the input voltage $V_{in}>V_{th}$, d=1; otherwise d=0. If the nonlinear errors such as op-amp nonlinearity and capacitor nonlinearity are not taken account in, the inter-stage transfer curve is linear and given by

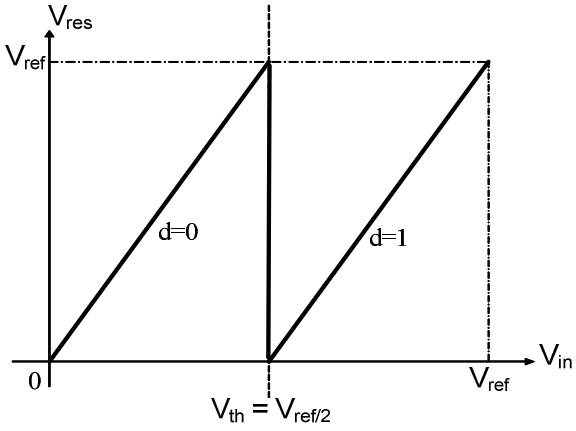
$$V_{res}=\frac{1}{1+\frac{1+\frac{C_2+C_{in}}{C_1}}{A_0}}\cdot\left[\left(1+\frac{C_2}{C_1}\right)\cdot V_{in}-\left(\frac{C_2}{C_1}\right)\cdot V_d(d)\right]. \qquad (6\text{- }1)$$

where A_0 is the op-amp dc gain, C_{in} is the input capacitance at the op-amp input node, and $V_d(d)=d\cdot Vref$ is determined by the output code d. Ideally if A_0 is infinite and C_1 and C_2 are exactly matched, we have:

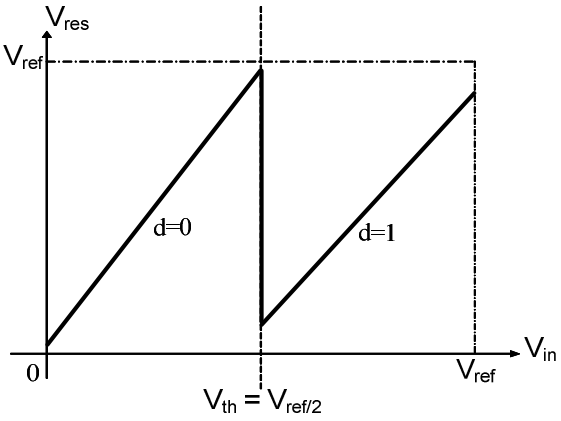
$$V_{res}=\left(1+\frac{C_2}{C_1}\right)\cdot V_{in}-\left(\frac{C_2}{C_1}\right)\cdot V_d(d)=2\cdot V_{in}-V_d(d). \qquad (6\text{- }2)$$

One ideal inter-stage transfer curve is depicted in figure 6-3(a). However, there are various errors that make the inter-stage transfer curve non-ideal. The comparator may have an offset

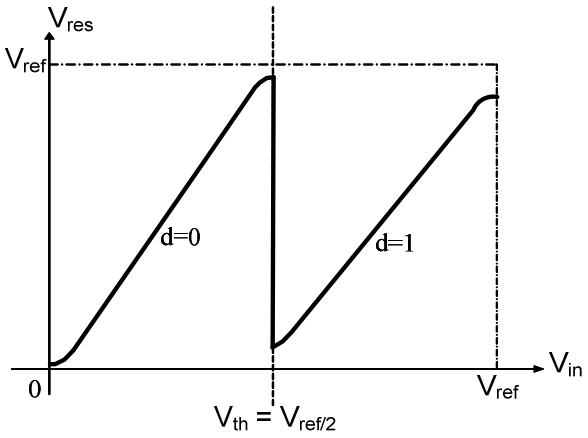
error such that $V_{th} \neq V_{ref}/2$. In actual situation, A_0 is finite, and C_1 and C_2 may not be perfect matched. The op-amp may also have input offset error. Besides, for over-range protection, the inter-stage gain is usually set to be less than 2 purposely. With above errors, the two pieces of inter-stage transfer curve are still straight but may deviate from the ideal position as depicted in figure 6-3 (b). Furthermore, there are also some nonlinear error sources such as the third order nonlinearity of the op-amp and the voltage coefficient of capacitance which cause the transfer curve bend a little bit as shown in figure 6-3(c). Both the linear and nonlinear errors should be removed by calibration. However, previous calibration algorithms usually can only handle the linear errors efficiently.



(a) Ideal Inter-stage Transfer Curve



(b) Ideal Inter-stage Transfer Curve with Linear Error



(c) Ideal Inter-stage Transfer Curve with Linear Error & Nonlinear Error

Figure 6- 3 -- Pipeline ADC Inter-Stage Transfer Curve Characteristics

The pipelined ADC performance is totally determined by the inter-stage transfer curve of each stage. To calibrate the ADC, we can just inspect and correct the errors of the transfer curves without caring about the detail error sources. Therefore, we need to characterize the transfer curves for calibration. The calibration performance will depend on the inter-stage transfer curve estimation.

Hardware calibration algorithms generally focus on correcting the source of the error in hardware by trimming or adjusting the hardware components that cause the error or by making hardware adjustments that mask the effects of an error. Digital calibration involves making changes in the incorrect raw output codes by ideally mapping an incorrect output code to a correct output code. Digital correction information is generally stored in some form of memory and some form of post processing of the raw output codes is generally required as part of the digital calibration approach. A good calibration algorithm should be capable of correcting both the linear and nonlinear errors in the ADC.

The Calibration, whether it is digital calibration or hardware calibration, requires training or learning period whereby the non-idealities of the ADC are determined and incorporated into the calibration algorithm. This calibration can be done in either the foreground or the background. In foreground calibration, a test or training sequence is applied to the ADC and calibration parameters are determined from this training period. With foreground calibration, the normal operation of the ADC is suspended. In background calibration, the calibration is accomplished in the presence of normal data flow through the ADC. With background calibration, the performance of the ADC will be degraded until the background calibration process is completed. Invariably periodic recalibration is necessary due to environmental changes that degrade performance. Most foreground calibration approaches are easier to implement than background calibration approaches but the latter are necessary in applications where an interruption of the data path is intolerable.

Numerous algorithms have been reported for ADC calibration in literature. For the most part, the hardware calibration was popular in the 1980's (such as Gray's algorithm for trimming the capacitors), while digital calibration has been dominating since the early 1990's. In the following part, some representative and frequently cited calibration algorithms will be reviewed and evaluated. The evaluation is focused on whether they accomplish the task of calibration and how effective the calibration is. Briefly, the evaluation will base on and the performance improvement and implementation cost. The performance improvement mainly refers the errors coverage, INL and DNL improvement. The cost defined here may include the implementation complexity, computation load and hardware overload such as memory size.

6.2.2 Reported Calibration Algorithms Review and Evaluation

6.2.2.1 Karanicolas and Lee Algorithm [1], [2]

This is a digital calibration algorithm and the paper introducing this technique is one of the most cited papers in the digital calibration field (61 citations by the SCI at the preparation of this paper). Many digital calibration algorithms reported recently are based on or similar with this algorithm. This algorithm was reported to be used on the pipeline ADC with the inter-stage gain equal to 1.93 to provide safety over range protection although this technique can be extended to the multi-bit per stage pipeline architecture. The original paper discussed this algorithm use two extra stage to achieve 15 bit resolution with the sub-radix gain. The calibration was done by keep the continuity of the overall input-output characteristic. To achieve this, the algorithm eliminated the discontinuity points in the pipeline inter-stage transfer curves. The basic idea is to make the inter-stage transfer curve continuous by interpreting the raw digital output codes correctly for each stage. As shown in Figure 6-4, for stage k, the inter-stage transfer curve is divided into two pieces by the transition voltage for the stage, V_{thk}. To make the transfer characteristics of stage k continuous, the calibration algorithm tries to measure the difference between the largest output code D_1 of the left portion of the transfer curve and the smallest output code D_2 of the right piece and then interprets the raw code "1" for the right portion of this stage as "D_1-D_2+1". In the first step of the algorithm, the un-calibrated tail stages of the converter, which were assumed to be ideal, were used to measure the discontinuity of the last stage (excluding those "ideal" tail stages) that was to be calibrated. Subsequent stages are calibrated sequentially by using the calibrated tail stages as seen from the stage under calibration to

estimate the discontinuity of the stage under calibration. This process is repeated until finally the first stage is calibrated at which time the calibration is complete and all the data was saved in a RAM. The basic ideal is shown in Figure 6-4 below:

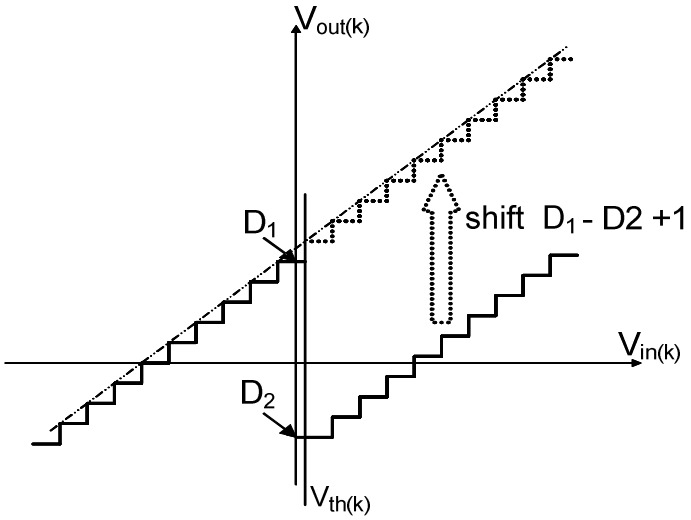


Figure 6- 4 -- Basic Ideal of the Karanicolas and Lee Algorithm

This algorithm is procedure-based with the implicit assumption that correcting discontinuities will calibrate the pipelined ADC but once the procedure is completed, there is no guarantee that the desired performance characteristics of the ADC, such as a required INL, DNL or SFDR specification, is achieved. The algorithm also requires the insertion of test signals at multiple points in the pipe thus disturbing the properties of the actual signal path. And the method of inserting zero input to define the major transient points is vulnerable with offset error, which means the major transient point may not happened exactly when input is zero. Also the discontinuous calibration also limited by the resolution of the following stage. As shown in Figure 6-5, due to the random offsets, the code width W_1 and W_2 are not controllable, and they may vary from 0 to 1 LSB. After the shift up and "connection", the code width around the major transition point is W_1+W_2, which may vary

from 0 to 2 LSB. Such kind of error can be accumulated along the whole pipelined data path, and then the total error after linear error correction may be not satisfying.

Another issue related to this algorithm is that this algorithm is sensitive to the nonlinear error in the pipeline inter-stage transfer curve caused by nonlinear errors in each block, such as the nonlinear mismatch of the capacitors, nonlinear gain of the inter-stage amplifier. The algorithm does not optimize the code mapping with such nonlinear errors present.

All those nonlinear errors will affect the calibration parameters (D_1 and D_2).

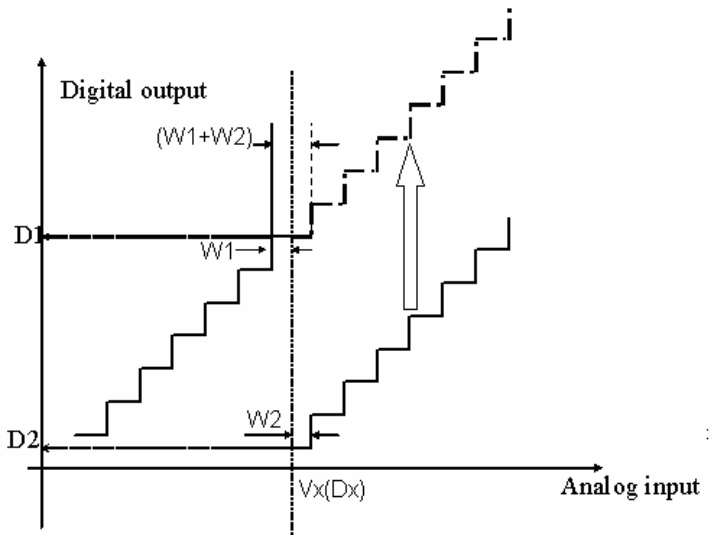


Figure 6- 5 -- Calibration code error in Karanicolas and Lee Algorithm

Since this algorithm only calibrated the few major transition points without knowing extra information for the whole transfer curve, the information gathered is not enough to guarantee the ADC performance. And this algorithm is procedure based, not output based, it does not provide the testing results of the ADC. The calculation complexity is reasonable low because only summation operation is required and the hardware overload is very small, only 132 byte memory is needed to store the calibration codes. This algorithm provides a very efficient

method to handle the linear errors and this work is very influential to many other calibration algorithms.

6.2.2.2 Soenen and Geiger algorithm [3], [4]

The basic concepts of the Soenen algorithm are very similar to those in the previous approach. The major distinction is that this calibration starts and in the use of wrapping in the calibration process whereby the output of the last stage is applied to the input of the first stage in a bootstrapped manner. Thus, in an n-stage pipeline, calibration can start at the last stage with the output of the last stage being applied to the input of the first stage. As with the previous algorithm, a test signal is applied to the stage under calibration and the measured digital outputs are used to remove discontinuities (i.e. decimate) in the transfer characteristics. In the implementation presented by Soenen, over-range protection was provided by what is often termed a "1.5 bit per stage" architecture in which an extra comparator was used in each stage. The performance limitations are essentially the same as those of the previous algorithm with the exception that the assumption of ideality of the tail stages is not made and with the exception that subsequent iterative calibration cycles can be used if further improvements in accuracy are required. There is another issue related to the bootstrapped manner. Under more and more stringent requirement of low power consumption tendency, scale-down technique is used to reduce the total power consumption and total die area. Thus driving ability will raise if the output of the last stage is being applied to the input of the first stage with the scale down from the first stage to the last stage. The load situation is different when adopting scale-down technique when wrapped architecture from the last stage compared with the normal connection and this difference will lead to the

error in calibration code and thus the calibration scheme cannot achieve expected results. Again, as mentioned in the previous section, this calibration needs the testing signal be inserted in the pipe and thus it will suffer from all kinds of nonlinearity error roused from pipe stages.

6.2.2.3 Ingino and Wooley algorithm [5]

This is a hardware-based calibration algorithm developed for the pipelined structure. The algorithm tunes the V_{th} and V_{refp} of each stage with the aid of an external high resolution DAC. For a pipeline structure, whether the decision interval slicing is ideal depends on two aspects. One is whether the slicing of each stage is ideal and the other is whether the inter-stage residue of each stage is correct. The algorithm attempts to achieve uniformly distributed transition points (or equivalently uniform interval slicing) by forcing the V_{th} of each stage to be exactly at the middle point of that stage's input range and by forcing the two segments of the residue transfer characteristics to precisely fit the input range of the following stage. It uses the exactly capacitor ratios of each stage to calculate the V_{th} and V_{refp}, which are unknown in reality and need to be calibrated for eliminating the mismatch error. In spite of the limitation of building high resolution DAC, which itself is a challenging work and highly area and design time cost, this algorithm will be limited by the factor that no real inter-stage transfer characteristic is ideal linear. In the presence of nonlinear inter-stage amplifier gain present, the residue transfer characteristics are nonlinear so no matter how the references or V_{th}'s are adjusted, the interval slicing for the following stages is not linear and major transition point will not locate at exactly in the middle of the whole range. Hence with nonlinear errors present, this algorithm will not provide uniformly distributed transition

points after calibration. This calibration algorithm is efficient with the linearity error, however, it is vulnerable to any sort of nonlinear effects and this is the same as Karanicolas algorithm. The hardware overload is high with the high resolution DAC and control loop.

6.2.2.4 Erdogan, Hurst, and Lewis algorithm [6], [7], [8], [21]

This is also a software-based digital calibration algorithm for the pipelined architecture. The basic idea is try to estimate the actual weight of each bit of the raw Boolean codes and then calibrate the codes using the estimated bit weight. The bit weight identification is accomplished by estimating the inter-stage gain using iterative calculations. The most-updated version of this algorithm also incorporates an estimate of the nonlinear gain error and includes this effect in the calibration code generation. This nonlinear error estimation is based on the assumption that the nonlinear error is due to the nonlinear op-amp gain and that the error has a bow shape. Several testing points have been inserted into the pipeline and the corresponding outputs are used to extract the linear and nonlinear coefficients in the predefined nonlinear model. So this algorithm is highly dependent on the accuracy of the nonlinear model and even moderate error in the model, such as some higher order nonlinearity that have been ignored in the model does appear, will results a big error in the final calibrated code. Therefore, such kind of calibration algorithm can be named as model-based calibration algorithm. Inclusion of a correction for nonlinearities is important for improving performance of the digital calibration algorithms but whether the proposed algorithm is sufficiently robust to amplifier model errors is less apparent and other nonlinear error sources such as capacitance nonlinearity affect the inter-stage transfer gain in a different way than the nonlinear op-amp gain. And for the second order open-loop

nonlinearities, the close loop form of the inter-stage transfer curve is mathematically difficult and thus the calibrated weight of each stage is hard to be calculated with few measured points.

In order to study this algorithm, several pipeline ADC circuits have been built up in different process using different architecture operational amplifier. From those simulations, we can see the nonlinearity is not necessary the second-order nonlinearity dominant. This nonlinearity cannot be control after fabrication with all kinds of process deviations. So designing the amplifier to achieve well shaped nonlinearity is also challenging work and this design is vulnerable to the process deviations and this weakness is discussed in detail in the following. Besides the difficulties of the modeling of nonlinearity of the opamp used to amplify the analog signal between each stage, there are some other possible nonlinearity error sources such as the nonlinearity from the switches, voltage dependence from the sampling capacitors. Nonlinear capacitor has been addressed in [22], [23], however, it is sensitive to the process and the temperature and cannot be predicted accurately in most schematic simulation level. So those error sources make the model-based calibration more vulnerable to the accuracy of the model itself. In the section 6.3, an original model-based calibration algorithm will be discussed. Even it has been carefully developed to relieve several limitations in [8], [21], the performance is not very encouraging with different amplifier design. The calculation complexity is high in order to estimate the nonlinear error parameters so the hardware load is correspondingly high.

6.2.2.5 Mayes algorithm [9]

Some of the best digitally calibrated results were reported by Mayes in 1996. Although his sampling rate for the ADC was comparable to what is now seen in over-sampled data converters, the performance of the algorithm does deserve attention and suggests significant improvements in performance with digital calibration algorithms can be achieved. The decimation used by Mayes is the same as used by Karanicolas and Lee as discussed above. As with other reported work using this algorithm, his performance with this algorithm was limited to about the 14-bit level and he attributed these limitations to nonlinear errors in the pipeline that are not calibrated with the decimation algorithm. He achieved 16-bit performance by adding a system-level nonlinearity correction algorithm in which he pre-characterized the nonlinearities in the process and then used a small ROM-based look up table addressed by the first few MSB of the decimated output to generate nonlinearity correction codes. These correction codes were then digitally added to the decimated output to generate the overall output. Although the pre-characterization for process variations is a non-conventional approach, he validated the concept for his process by using the same correction codes for wafers coming from 5 wafer runs from 4 processes. The cost for this algorithm is the large volume of the digital hardware overload because there are many testing points to characterize the system level nonlinearity of the pipeline and so are the nonlinear correction codes. This work suggests that on-chip digital calibration can be extended to higher resolution levels and higher frequencies if the static nonlinearities in the ADC can be managed. Also his work proves that the calibration will be more robust if no pre-defined model was involved and this provides the possible solution for any future pipeline ADC that needs to achieve over 14 bit performance.

6.2.2.6 Several Other Calibration Algorithms

Besides the five representative algorithms discussed above, there are several other algorithms that have been used for pipelined ADC calibration. Gray, [10] et. al. used capacitor trimming to compensate for finite gain errors in the inter-stage amplifiers. This is a hardware-based calibration approach. Song has also concentrated on measuring the inter-stage transfer gain errors and used digital calibration to compensate for the discontinuity errors in the pipeline caused by the gain errors [11], [13]. Opris, et. al. [14], [15]and Chuang [17] et.al. used the same basic idea used in the Karanicolas approach . Allstot et. al. [18], [19] at ISCAS 2003 pointed out that even the discontinuity correction (decimation) in the Karanicolas algorithm is affected by nonlinear errors in the pipeline and proposed an improvement to the Karanicolas algorithm that offered improvements in the decimation. In their works, a highly linear DAC was used as a signal source to find the actual major transition points of the ADC and from these measurements they were able to generate the decimation correction codes. The practicality of generating the highly linear excitation needing for calibration was not addressed and although they pointed out the nonlinear errors, the decimation algorithm does not calibrate for the nonlinear errors.

6.3 An Original Model-Based Calibration Algorithm

In the section, an original model-based calibration algorithm is presented. This algorithm is similar with Lewis algorithm [8] and [21], however, several problems which has been overlooked in Lewis work have been carried out here.

6.3.1 Reverse Transfer Function Estimation

As we mentioned in the above, the linearity of the ADC will be very good if the digital output code can be interpreted correctly. For model-based calibration algorithm, the nonlinearity is assumed mostly comes from the nonlinear transfer function of the residue amplifier, which is used to amplify the analog signal along the pipe of stages. Because it is mathematically difficult to solve the reverse transfer function for the nonlinear model even with the second order nonlinearity inherent in the amplifier, to find an efficient and practically useful method to estimate the reverser transfer function is necessary.

In Figure 6-6, a simple model for the residue amplification stage of pipeline ADC is shown.

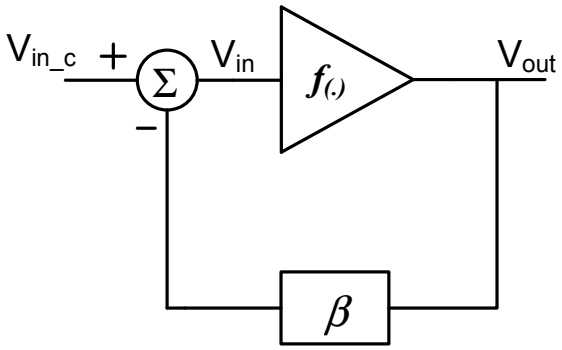


Figure 6- 6 -- Simple Model for Residue Amplification Stage.

For open loop gain transfer function, $f_{(.)}$, it is assumed that it will achieve high gain for linear relationship with two ends bend due to the nonlinearity saturations. We will use two figures below to do the approximation of the reverse transfer curve.

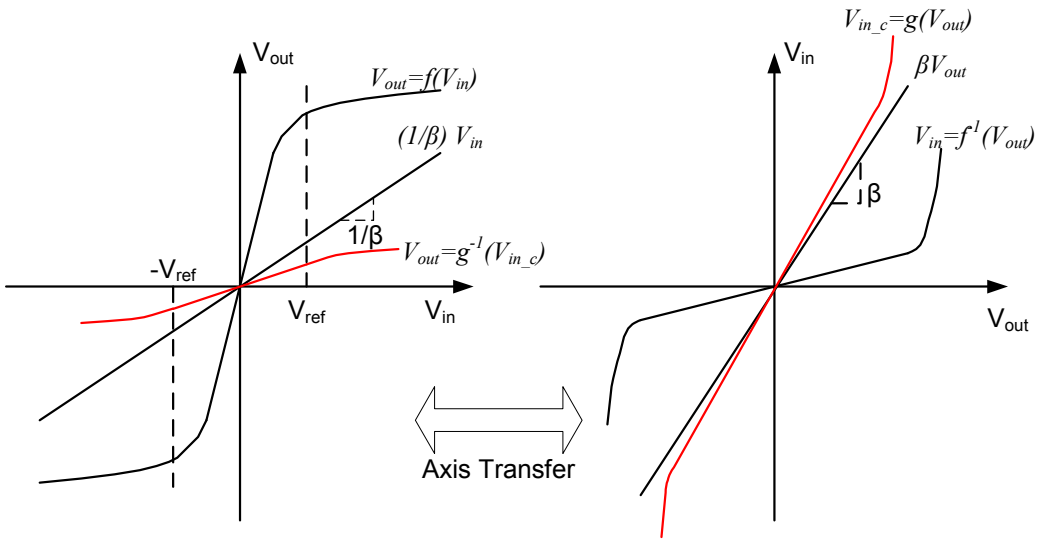


Figure 6- 7 -- Axis Transfer to Find the Approximately Reverse Transfer Function

As shown in Figure 6-6 and Figure 6-7, the forward transfer function can be expressed as:

$$V_{out} = f\left(V_{in\_c} - \beta \cdot V_{out}\right). \tag{6- 3}$$

$$V_{in\_c} = f^{-1}\left(V_{out}\right) + \beta V_{out}. \tag{6- 4}$$

In order to find the reverse transfer function, we can consider V_{in_c} as the combination of two curves: the straight line transfer function representing the linear relationship, βV_{out}, and the nonlinear component: $f^{1}(V_{out})$. For more convenient analysis, the axis transfer can be taken to result the figure in the right side of Figure 6-7. The straight line $(1/\beta)V_{in}$ will map to the straight line: βV_{out}. And we know the nonlinear line $f(.)$ contains the high magnitude linear part with two ends bend over for the amplifier operation common wisdom, so the mapping nonlinear curve, $f^{1}(V_{out})$ will be contains a low slop straight line with the both of two ends bend upward. If we write the equation:

$$V_{in\_c} = f^{-1}\left(V_{out}\right) + \beta \cdot V_{out} = g\left(V_{out}\right). \tag{6- 5}$$

Then the reverse transfer function, *g(.)* will be the combination of two curves; nonlinear curve $f^{1}(.)$ and straight line with the slop of value β. Therefore, *g(.)* will be shown as the red line with the characteristic of a very close to straight line around the middle of the full range and two ends bend upward gradually in the right side plane. We can also map this *g(.)* back to the forward transfer curve plate which is draw as the red line in the left side of Figure 6-7. We can use the simplest nonlinear mathematic model to describe those two curves as:

$$V_{out} = \frac{1}{\beta} V_{in\_c} - \frac{1}{A} V_{in\_c}^{3}. \qquad (6\text{-}6)$$

This implies that the amplifier nonlinear transfer function contains a nonlinear component modeled by 2nd order harmonics. In the following section, we will notate linear coefficient as g_0 and nonlinear coefficient as c_0, which represent $1/\beta$ and $1/A$ in (6-6).

6.3.2 The Model-Based Calibration Algorithm Development

For high resolution Pipeline ADC, both linear and nonlinear error should be corrected for high linearity. The nonlinear part comes from nonlinear open-loop gain of the residue amplifier, nonlinear voltage coefficient of capacitors, switches in the signal path, etc. Isolating each nonlinear source and correcting it independently will be very hard and unnecessary. This new method looks each single stage as an independent cyclic ADC and tries to correct the both linear and nonlinear error without isolating the error sources. Because residue amplifier is always used as close-loop format, we model the close-loop input-output relationship of a cyclic stage and calibrated the interpretation of the ADC output code for linear and nonlinear errors.

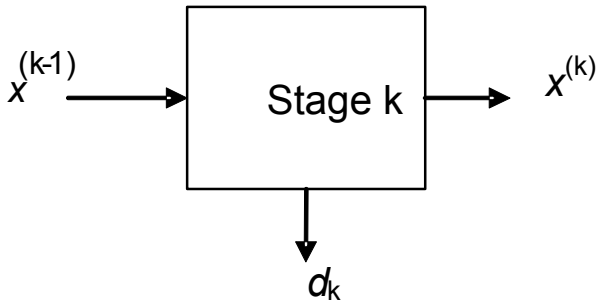


Figure 6- 8 -- Block Diagram of Single Pipe State

The transfer characteristic of a cyclic stage can be modeled as

$$x^{(k)} = a \cdot \left(x^{(k-1)} - d_k \cdot \frac{v_{ref}}{2} \right) - b \cdot (x^{(k-1)} - d_k \cdot \frac{v_{ref}}{2})^3 . \qquad (6\text{- }7)$$

From the experience in the circuit design, the nonlinearity in the transfer characteristic is generally a decreasing function and equal to 0 at 0. For simplicity, the nonlinear term is chosen to be a third order polynomial in (6-7). The true nonlinearity can be pretty much different and with some higher component. But we believe the most critical part should be the third part as we analysis in the previous section. The main ideal is trying to extract the linear and nonlinear coefficients from the output data and improve the linearity of the final output.

The interpretation of the ADC output code with a simple step of nonlinearity calibration can be written as

$$\begin{aligned} x^{(N-1)} &= d_N \cdot \frac{v_{ref}}{2}, \\ x^{(k-1)} &= \frac{1}{g} x^{(k)} + c \left(x^{(k)} \right)^3 + d_k \cdot \frac{v_{ref}}{2}, \quad k = 1,2..., N-1. \end{aligned} \qquad (6\text{- }8)$$

The input to the ADC associated with a specific output code can be determined by (6-8). From that we can define a function *b* as

$$x = x^{(0)} = b(g, c, d_1, d_2, ...d_N). \quad (6\text{-}9)$$

In (6-9), g represents the linear gain coefficients, and c characterizes the nonlinear error. If we have accurate values of g and c we can recover the input voltage from the output digital data with good linearity.

As a first step, we capture two output codes with the same input voltage at about 0 but d_1 set to be *0* and *1*, respectively. Then we define a function of g and c as

$$f_1(g, c) = b(g, c, 0, d_2^{(0)}, ...d_N^{(0)}) - b(g, c, 1, d_2^{(1)}, ...d_N^{(1)}). \quad (6\text{-}10)$$

The optimal values of g and c will make the function equal to 0, which means the gap between the major transient points should be 0.

$$f_1(g_0, c_0) = 0. \quad (6\text{-}11)$$

Setting the function f_1 to be 0, we get a curve on g-c plane which contains the point (g_0, c_0), but this is not enough for find both g and c. So we need to build another function with other measurements.

The input points $(-3/4)V_{ref}$, $(-1/4)V_{ref}$ and $(1/4)V_{ref}$ are chosen for building the second function. The accuracy of those nominal values is not important and what needs to be accurate is the relative accuracy. The reason to choose those three points is that we want to the points across the MSB and the second MSB transient points. And the output of those points will contain nonlinear error information. If the symmetrical measuring point, such as $(-3/4)V_{ref}$ and $(+3/4)V_{ref}$, are chosen as [21], the data will not be helpful to identify the nonlinearity coefficients if two sides are identical. This also can be analyzed in Figure 6-9. If the left side and right side are identical, the vertical distance between $+¾V_{ref}$ to $+ ¼V_{ref}$ will be the same no matter if the transfer curve is linear or nonlinear. Thus this cannot be used to

extract the nonlinearity coefficients. However, if asymmetrical testing points are set up as shown in this work, only when the two pieces of transfer curved being calibrated to straightly line, the vertical distance between the –¼ V_{ref} and +¼ V_{ref} and the one between the –¾ V_{ref} and –¼ V_{ref} would be the same.

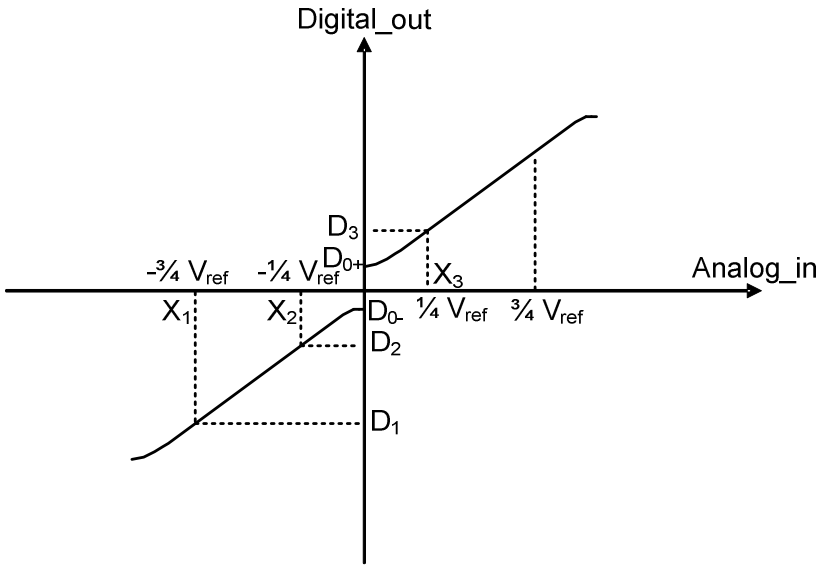


Figure 6- 9 -- Measuring Points Set Up

From above figure, we can see that inputs X_1, X_2 and X_3 have the same distance between each other, while the output will not have the same distance due to the linear and nonlinear error. If we can somehow extract the linear and nonlinear error and recover the input from output D, then the distance between the recover input X'_1, X'_2 and X'_3 will be the same. This will lead to the second equation as shown below:

$$f_2(g,c) = [b(g,c,D_3) - b(g,c,D_2)] - [b(g,c,D_2) - b(g,c,D_1)]. \qquad (6\text{- }12)$$

We can show that

$$f_2(g_0,c_0) = 0, \qquad (6\text{- }13)$$

So setting the function f_2 to be 0 gives another curve on g-c plane that contains the point (g_0, c_0). Putting the two equations together, we have

$$\begin{aligned} f_1(g,c) &= 0, \\ f_2(g,c) &= 0. \end{aligned} \tag{6- 14}$$

The solution to the (6-13) gives the point (g_0, c_0). We can use iteration to find this solution as

$$\begin{bmatrix} g_{k+1} \\ c_{k+1} \end{bmatrix} = \begin{bmatrix} g_k \\ c_k \end{bmatrix} + \begin{bmatrix} 0.1 & 0 \\ 0.1 & 0.1 \end{bmatrix} \begin{bmatrix} f_1(g_k,c_k) - f_1(g_0,c_0) \\ f_2(g_k,c_k) - f_2(g_0,c_0) \end{bmatrix}. \tag{6- 15}$$

Each stage of pipeline ADC can be considered as a cyclic ADC and both linear and nonlinear errors can be calibrated with the algorithm described above. Thus we can use those coefficients to recover the whole digital output of the pipeline ADC to get better linearity. It is important to note here that those two coefficients have to be solved simultaneously with Newton iteration equations sets as (6-14). Unless those two coefficients are totally uncorrelated, can they be solved individually and that will bring more calculation errors into the calibration algorithm [21].

6.3.3 Simulation Results

6.3.3.1 MATLAB Model Simulations

The Matlab pipeline ADC model is used to verify this calibration algorithm for the first step including random gain errors, random reference offsets, random opamp offset and random DAC offsets. The amplifier models is assumed to be second order nonlinearity dominant and achieve a bow shape gain versus the output voltage. The simulation runs for different resolution levels with different nonlinear errors.

For 14 bit level, with nonlinear error $c = 2^{-6}$, non-calibrated INL is 15.5 LSB. The INL will be reduced to 2.8 LSB with liner gain calibration and to 1.2 LSB with both linear and nonlinear errors being calibrated. The simulation results are shown below.

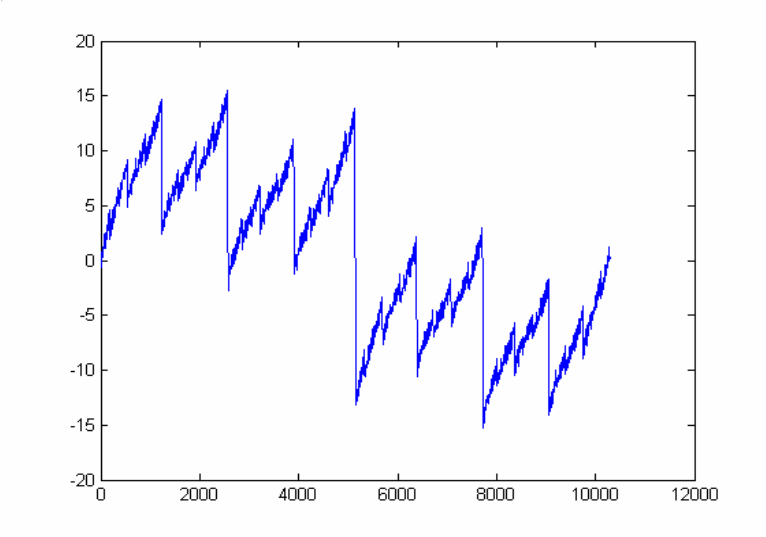


Figure 6- 10 -- Non-Calibrated INL of 14-bit Pipeline ADC

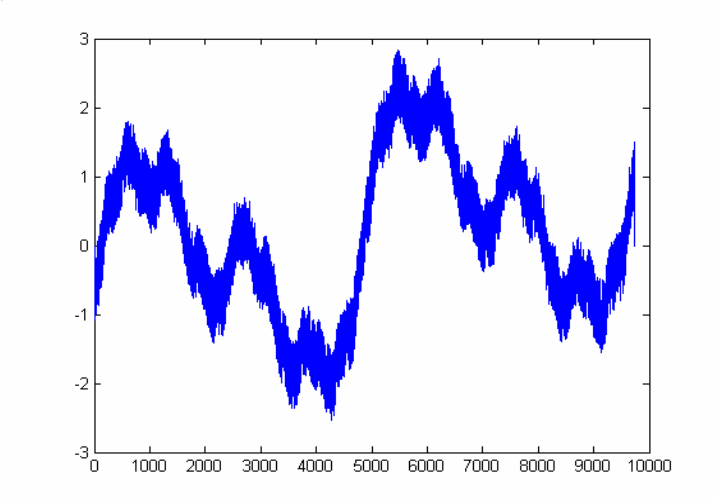


Figure 6- 11 -- Linear Calibrated INL of 14-bit Pipeline ADC

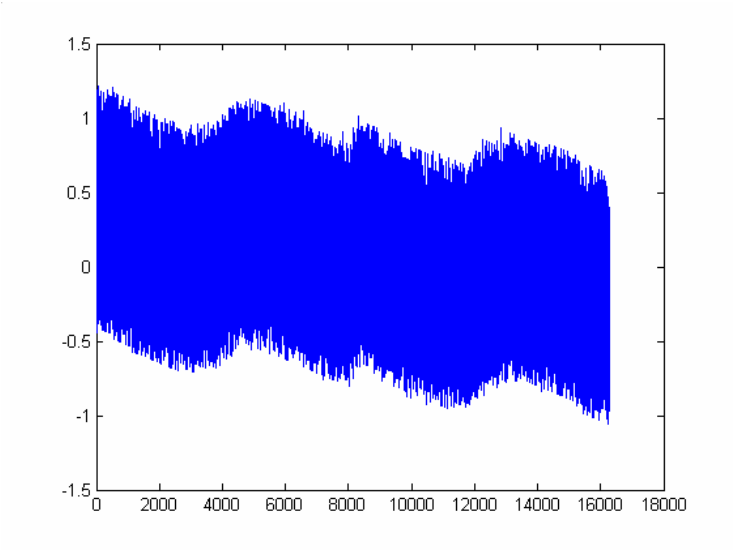


Figure 6- 12 -- Linear Plus Nonlinear Calibrated INL of 14-bit Pipeline ADC

The Matlab simulation results for 16 bit level are shown in Figure 6-13 to Figure 6-15.

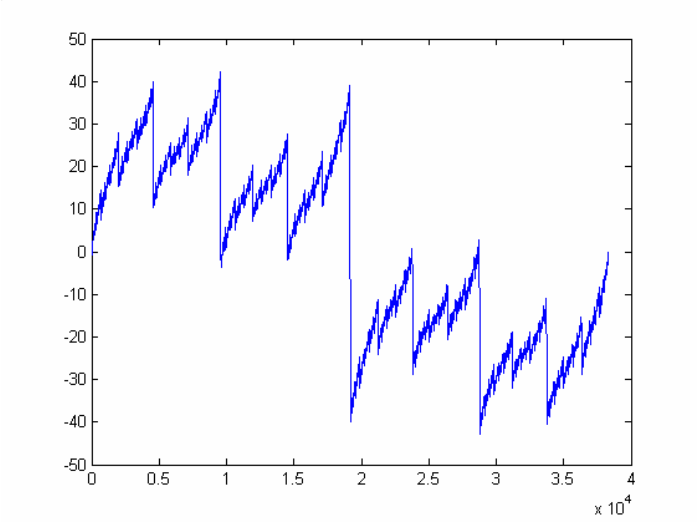


Figure 6- 13 -- Non-Calibrated INL of 16-bit Pipeline ADC.

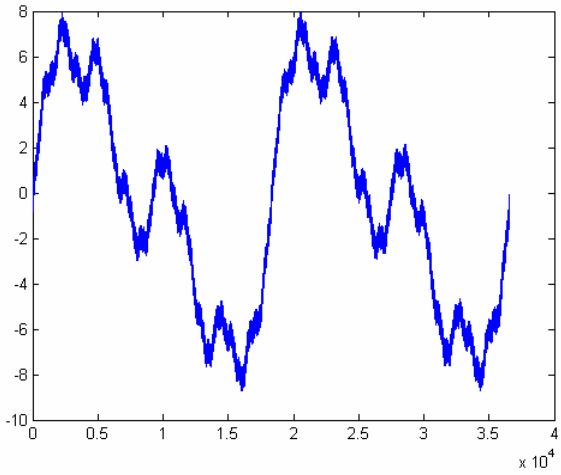


Figure 6- 14 -- Linear Calibrated INL of 16-bit Pipeline ADC.

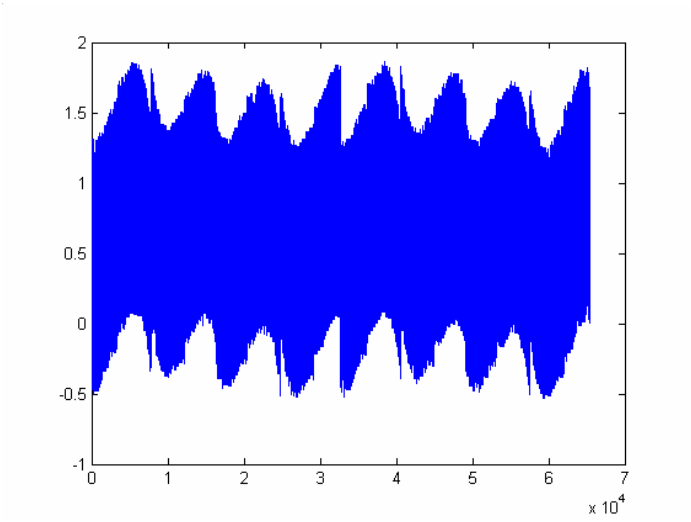


Figure 6- 15 -- Linear Plus Nonlinear Calibrated INL of 16-bit Pipeline ADC

Simple Table will summary the simulation results.

Table 6- 2 MATLAB Simulation Summary

Resolution (bits)	INL (LSB) w/o Calibration	INL (LSB) w Linear Calibration	INL (LSB) w Linear + Nonlinear Cali.
14	15.5	2.8	1.2
16	41	8.7	1.8

From Table 6-2, it is very convincible that this calibration algorithm not only can remove the linear error but also very efficiently eliminate the nonlinearity and the performance is potential to reach at 16 bit level with this new calibration algorithm.

However, reminding that the MATLAB model only contains the nonlinear errors predicted by the analysis derived in the section 6.3.2 and it contains no real information about the real amplifier nonlinear transfer characteristics. So the simulation only proves that this algorithm will be very effective if and only if our non-linear model is accurate. In order to investigate the robustness of this algorithm, a pipeline ADC has been built up with different kind of opamp and that is the topic of the next section.

6.3.3.2 Transistor Level Simulations

As we mentioned above, different opamp architectures are used in the transistor level pipelined ADC to testify the robustness of the proposed model-based calibration algorithm. The pipeline ADC adopted the 1 bit/ stage structure as shown in Figure 6-2. The major building blocks will be described briefly in the following part.

Boost-Strap Switches

The switches are implemented using boost-strap switches as introduced in [24]. The reason for choosing this boost-strap switch is that the nonlinearity due to the input dependency of the normal switches cannot be modeled by a simple 3rd order term as shown in (6-6) and it has to be minimized to focus on the nonlinearity associated with the opamp. The concept and the practical schematic design are shown in Figure 6-16.

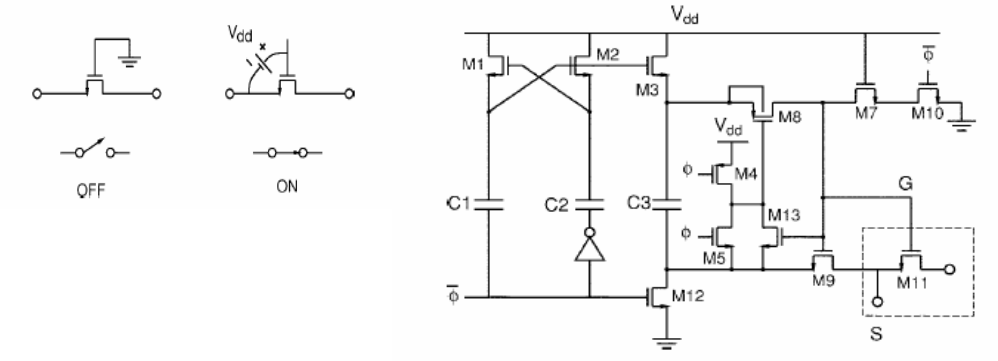


Figure 6- 16 -- Boost Strap Switch

In the "off" state, the gate is grounded and the device is cutoff. In the "on" state, a constant voltage of V_{dd} is applied across the gate-to-source terminals, and a low on-resistance is established from drain to source independent of the input signal. The actual circuit of bootstrapped switch operates on a signal phase clock ϕ that turns the switch M_{11} on and off. In the off phase $\bar{\phi}$, M_7 and M_{10} are conducting, the gate of M_{11} is connected to the ground, switch is off. At the same time, M_3 and M_{12} are conducting, M_8 and M_9 are isolated, therefore the voltage of C_3 is charged to V_{dd}. In the on phase ϕ, M_8 and M_9 are conducting, M_3 and M_{12} are cutoff, therefore the voltage of C_3 is applied to the gate and source terminals. In the actual circuit, M_1, M_2, C_1, C_2, and the inverter form a clock multiplier (voltage booster), that enables M_3 to uni-directionally charge C_3 during the off phase. M_4 and M_5 control the gate voltage of M_8, in the phase $\bar{\phi}$, M_4 connects the gate of M_8 to the ground, therefore M_8 is

cutoff; in the phase ϕ, firstly M_5 connects the gate of M_8 to a voltage nearly ground and enables the bootstrapped circuit. The body of M8 is tied to its source, latch-up is suppressed. C_3 must be sufficiently large to supply charge to the gate of the switching device in addition to all parasitic capacitances in the charging path. If C_p is total parasitic capacitance connected to the top plate of C_3, then $Vg = Vs + \frac{C3}{C3+Cp} Vdd$. After carefully design this switch, the nonlinearity associated with it can be neglected.

Comparator

The comparator is shown is Figure 6-17. The latch signal will enable this dynamic comparator. The major design specification for this pipeline ADC with calibration algorithm is the offset voltage. The error due to the over range problem caused by the offset voltage is unrecoverable with this algorithm so that the comparator is required to produce the offset voltage will not set the analog output over range.

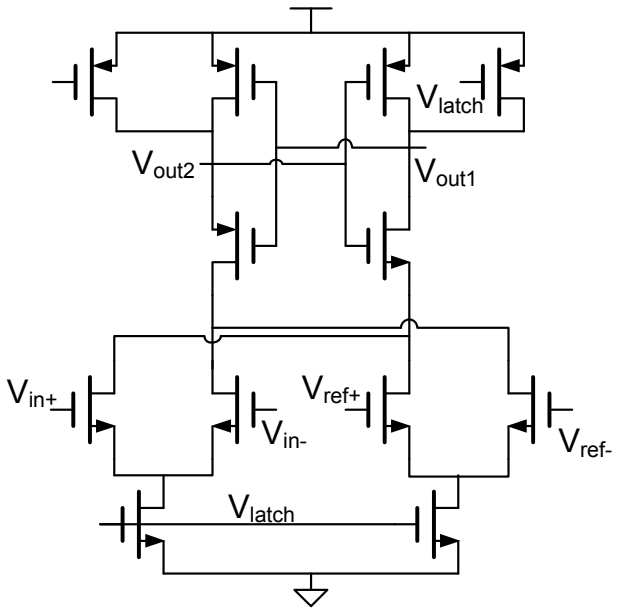


Figure 6- 17 --Dynamic Comparator

Residue Amplifier

In order to focus on the nonlinear calibration algorithm robustness to the model errors, there are total three different architectures op amp has been used in this pipeline to verify this algorithm. Since the most nonlinearity errors comes from the first several MSB stages and especially in the multiple bit per stage structure, which provides higher power efficiency and is adopted as a popular structure in pipeline ADC architecture, the linearity performance is highly rely on the first stage, we will concentrate on the comparison on the residue signal linearity characteristics before and after the linear and nonlinear calibration for different opamp structures. By following the residue analog signal with infinite resolution of ideal ADC, the quantization errors will be removed. The INL will be normalized to 16 bit level.

The first opamp structure is simple two stage amplifier as shown in Figure 6-18.

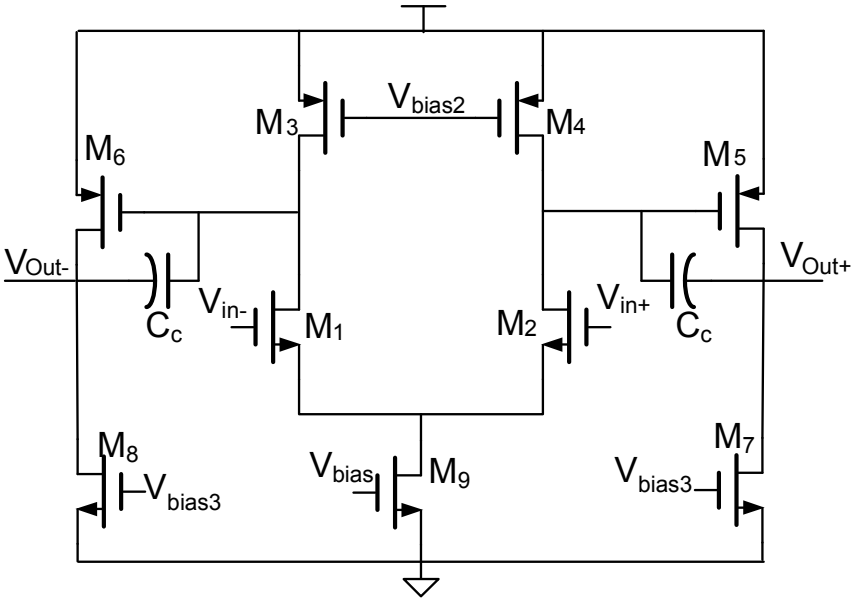


Figure 6- 18 -- Simple Two Stage Amplifier

This amplifier has moderate high open loop gain and simple structure. As we discussed before that the higher the open loop gain the better close-loop linearity with

feedback structure. The simple miller compensation capacitor is used to stabilize this opamp. The non-calibrated INL is shown below:

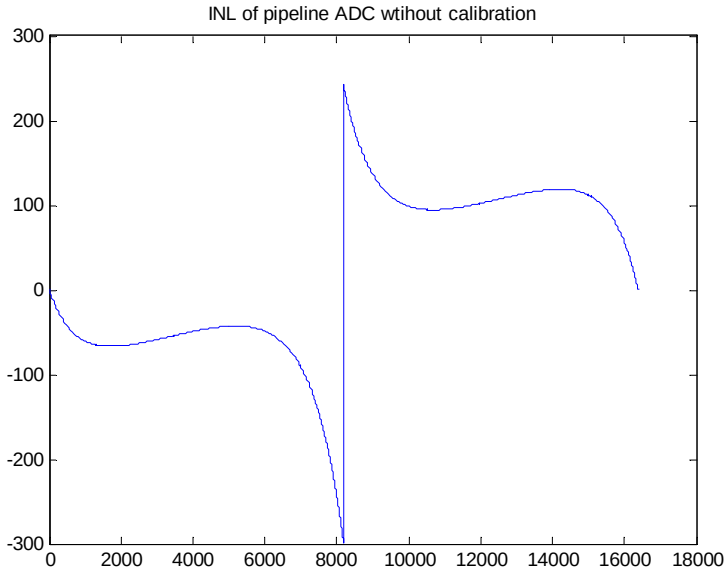


Figure 6- 19 -- Non-Calibrated INL

We can see that due to the moderate gain and linearity, the INL of this pipeline ADC is about 300 LSB, which equivalent to 7.5 bit level. After the linearity calibration, the discontinuous point has been removed and the INL plot is shown in Figure 6-20 below.

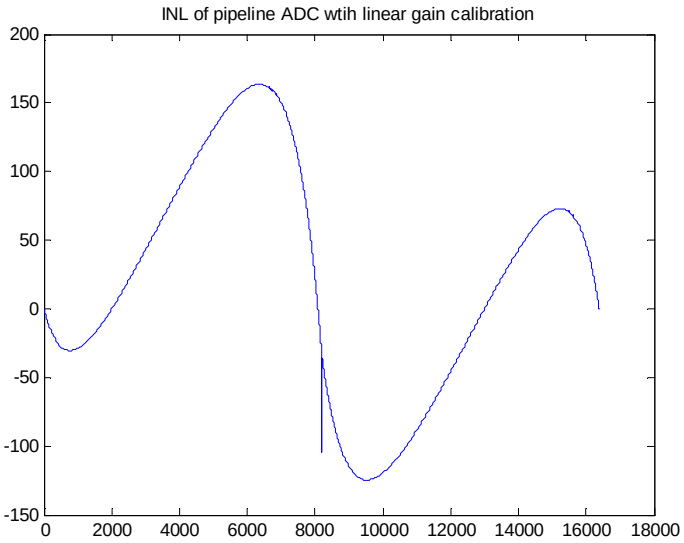


Figure 6- 20 -- INL with Linear Calibration

With the linear Calibration, the major error left is the nonlinearities and linear calibration improved the ENOB to 9 bit level. The INL plot after both linear and nonlinear calibration is shown below.

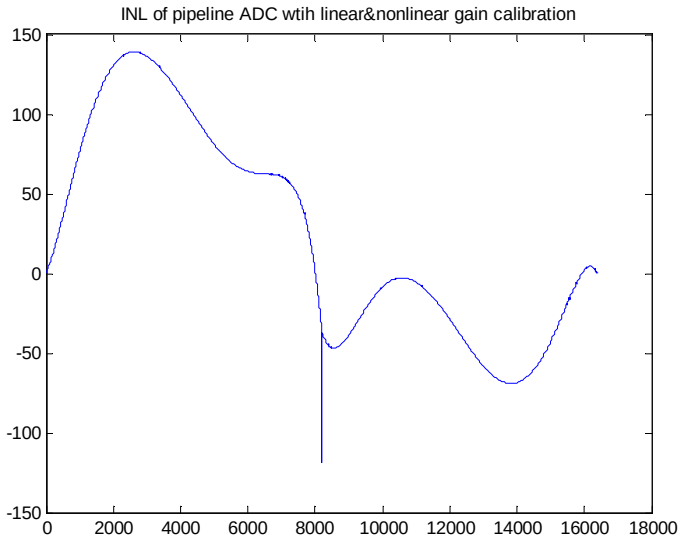


Figure 6- 21 --INL after Linear and Nonlinear Calibration

The INL of nonlinear calibration has been improved with about 24 LSB so the pipeline ADC achieves around 10 bit ENOB. Although nonlinear calibration improved the ENOB by about 1 bit by remove some nonlinear errors, there is still significant nonlinearities left and they are not eliminated by the nonlinearity calibration because they cannot characterized by the simple 3rd order nonlinear model described in (6-6). This calibration algorithm is actually trying to improve the linearity by adding some nonlinearity erros according to the pre-defined models to compensate the original nonlinearity. Therefore if the model is not accurate, the nonlinearity errors being added into the final results will not just only invalid to compensate the nonlinear error, but furthermore will deteriorate the overall linearity performance. So the nonlinear calibration algorithm based on a simple 3rd order nonlinear transfer function can only achieve 10 bit ENOB performance with this simple two stage opamp.

The second amplifier inserted in this pipeline ADC is folded-cascode amplifier shown in Figure 6-22.

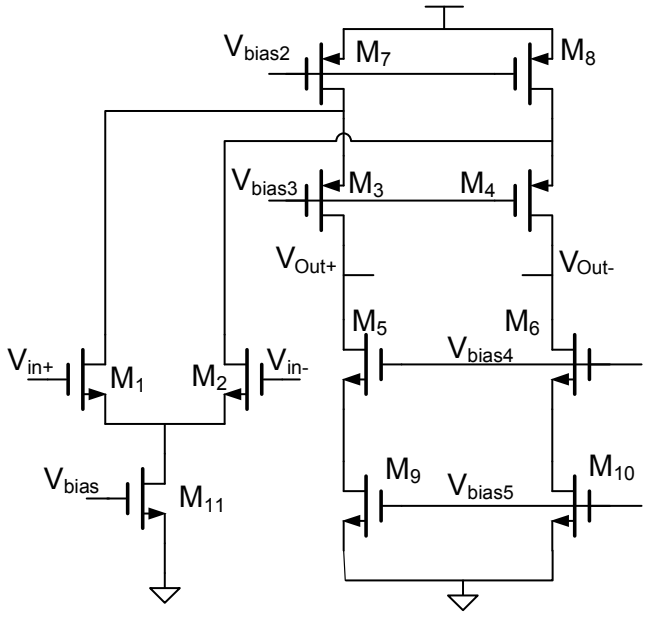


Figure 6- 22 -- A Folded-Cascode Amplifier

Compared with the simple two stage opamp, this folded-cascode opamp offers higher DC gain. The INL without calibration, with linear calibration and with both linear and nonlinear calibration are shown in Figure 6-23 to Figure 6-25.

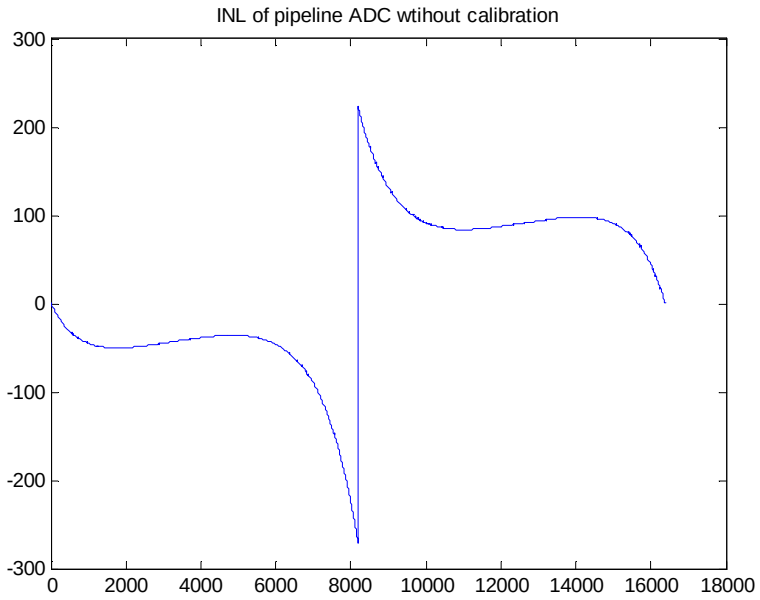


Figure 6- 23 -- INL with No Calibration

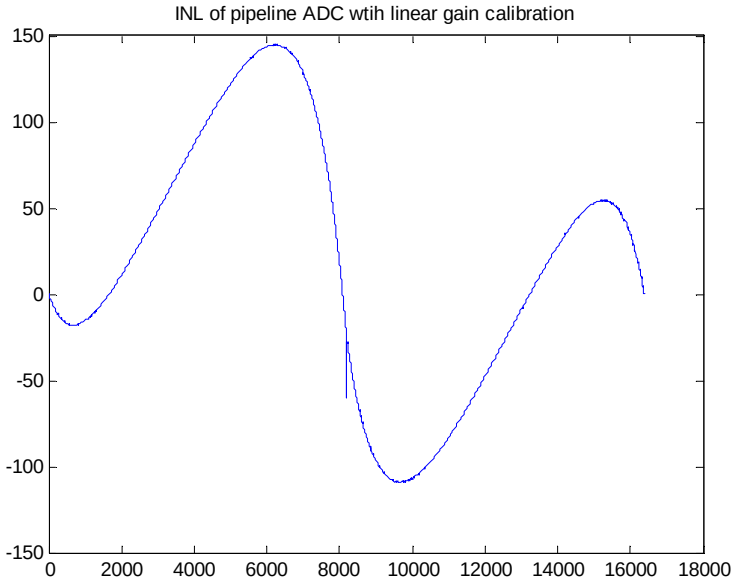


Figure 6- 24 -- INL with Linear Calibration

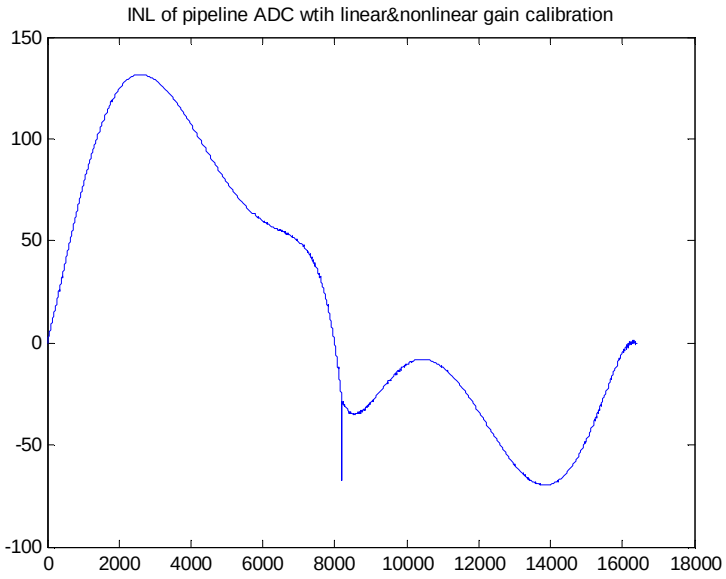


Figure 6- 25 -- INL with Linear and Nonlinear Calibration

It is clearly shown that the folded cascode amplifier provides very limited improved linearity and the ENOB without any calibration is about 8 bit. The linear calibration reduced the INL to about 145 LSB level. However, the same observation has been made with this nonlinearity calibration that with simple 3rd order models, this calibration cannot remove major part of the nonlinearity errors and cannot provide expected performance.

The next step, the pipeline is simulated with a telescope cascode two stage amplifier, which provides very high open loop and the better linearity is expected.

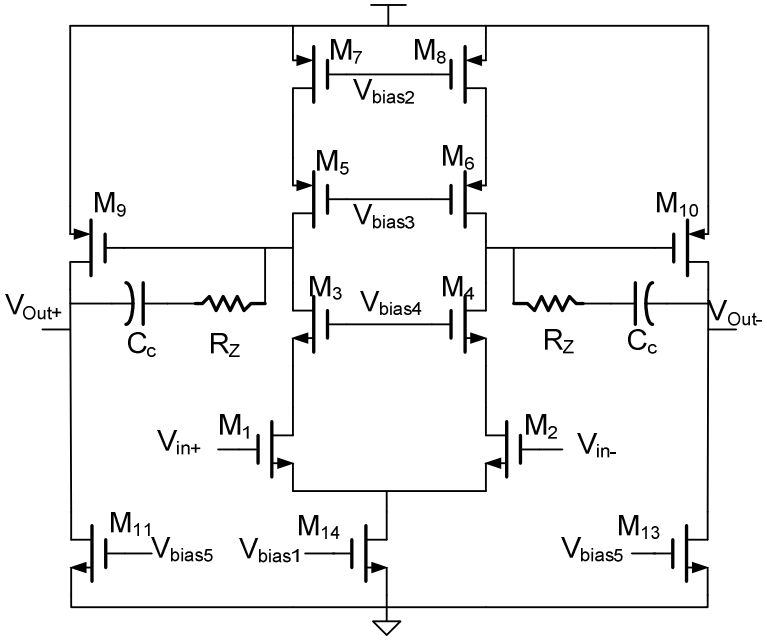


Figure 6- 26 -- A Two-Stage Telescope Cascode Amplifier

The INL plot with no calibration is shown below.

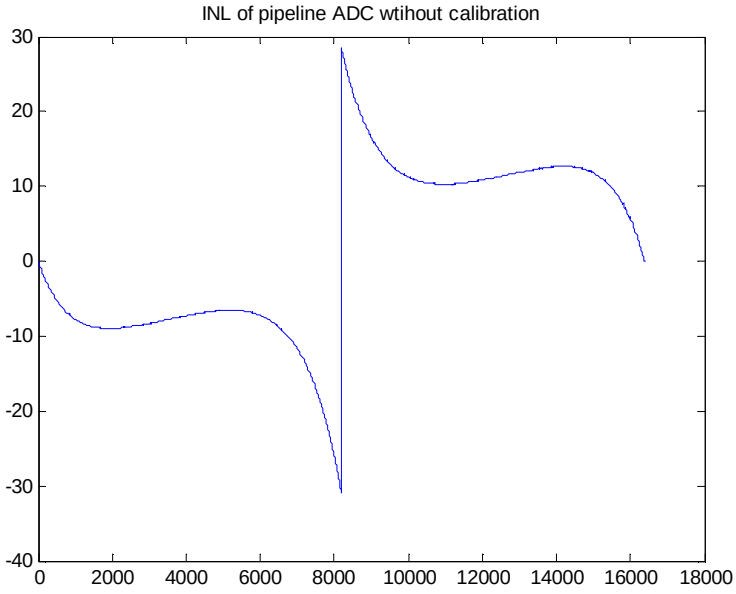


Figure 6- 27 -- INL with No Calibration for 16-bit Level

We can see that this telescope two stage amplifier provides much better linearity and the ENOB without any calibration is about 11 bit. The linearity calibration has removed the discontinuity as before.

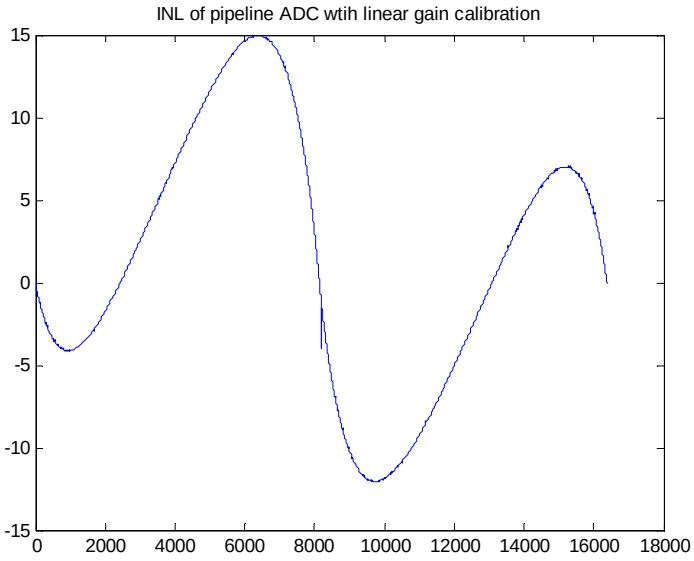


Figure 6- 28 -- INL with Linear Calibration for 16-bit Level

The linear calibration reduced the INL from 30 LSB to 15 LSB and we can see the nonlinear components left are similar with what exhibited in Figure 6-20. So the nonlinear calibration will be limited by the accurate of the nonlinear model used to describe the transfer characteristics and the performance after the nonlinear calibration is not expected to be efficient.

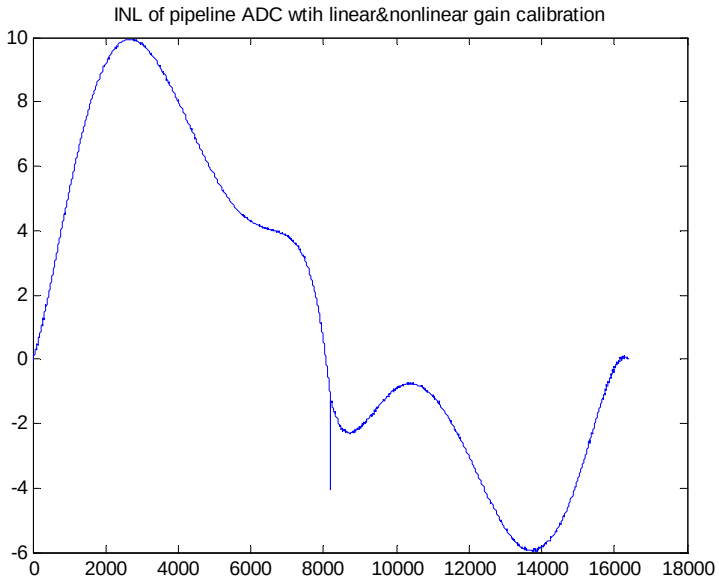


Figure 6- 29 -- INL with Linear and Nonlinear Calibration for 16-bit Level

In Figure 6-29 exhibits that the nonlinear calibration improved the linearity by about 1 ENOB. If we check the highest INL which limited the linear performance of this ADC, we can find that those errors are actually what we added for compensating nonlinearities described by the model (6-6). Therefore, only when the nonlinearity model we built matches characteristics the inter-stage transfer curve very well, this model-based calibration algorithm will eliminate the nonlinear errors very effectively, such as simulations shown with MATLAB models. If any considerable mismatch appeared between the pre-defined model and practical transfer curve, which is very likely happen with fabrication circuits, this model-based calibration algorithm will not be productive to remove all the nonlinearities and its performance really rely on the amplifier architectures. In some cases, this model-based algorithm will even add more nonlinearities to deteriorate the performance if the model doesn't match the transfer curve at all.

6.4 Conclusion

In this chapter, a comprehensive study of the existing calibration algorithms has been discussed. Several popular calibration algorithms have been analyzed and the major

contributions and the limitations and costs have been addressed and evaluated. From our study, we can see that most calibration algorithms are vulnerable to the nonlinear errors in the pipeline ADC. Nonlinear error will make the models not accurate and thus affect those algorithm strongly depend upon the stage model. Some algorithm needs high accurate high linear DAC and thus will increase the cost of the ADC design because it is challenge to build those extra high performance DACs. The review and comparison of those calibration algorithms is most targeted to find the major limitations of the pipelined ADC. Based the analysis of those calibration algorithms, it is attracting to develop a algorithm that is not sensitive to the inter-stage model and can handle nonlinear error and that algorithm can be predicted to improve the pipeline ADC impressively.

From section 6.3, with both MATLAB models and transistor level models and simulation, it has demonstrated that the model-based algorithm strongly dependent on the accurate of the model and it is very hard to be controlled with the different amplifier architectures, process and temperature variations. Besides those amplifier nonlinearities, there is some nonlinearity existing in the capacitance and has not been included in those simulations. So the real fabricated circuits are more complicated and even harder to be described with some simple models. Unless a very complicated high order model has been involved to describe the transfer behavior of the pipeline inter-stage transfer curve, the model-based calibration algorithm will be very vulnerable to any model errors and in some cases it will even deteriorate the overall linearity performance. However the extra hardware and digital computing load for solving high order complicated models will be significantly increased. Of course, building an opamp to match simple 3rd order nonlinear function is a possible option. But designing such an opamp itself will be a challenging job and somehow it

may be even harder to design a high gain high linear opamp, such as shown in the last opamp structure. We conjecture that is why there is very few or even any existing nonlinear calibration algorithm has been adopted in commercial products even though this is hot topic and under the spot light for over 20 years. The solution now relies on the calibration which does not rely on the pre-defined models, which we called the output-based calibration algorithm [25], [26], [27].

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CHAPTER 7 SUMMARY

My colleagues and I are focus on the high linearity analog and mixed-signal integrated circuit design. Our research involves several domains; the high linearity analog filter with applications in low frequency, high linear transconductance networks study when inserted in feedback systems, area optimization for active filters, linear current division circuit principle investigation and the low power small area current division D/A converter design, Calibration algorithms of pipeline ADC for improved static linearity.

We develop a technique that using a passive transconductance networks in the traditional active filters for low frequency applications. In this new strategy, the filters can benefit the high linearity from the passive components with a very limited silicon die area. The prototype circuit has been fabricated with standard CMOS process and the experiment results support our design and analysis. Beside this implementation, the further study of the transconductance networks relationship with the opamp design, circuit linearity, noise and the process variations have been investigated and the close form expressions demonstrate the trade off between the area efficiency and the other circuit specifications. Also the simulation the testing results show highly agreements with our analytical works.

Another contribution of our works is to study a well-recognized and very influential current division circuit. Our study shows that the original claims were misleading and the all the reported experimental verified the works are actually based on other more general circuitry principle. However, a novel low power current division DAC was invented based on this technique with very small active area and the simulation results show a very promising applications for this approach in low and media resolution, high speed, small DAC designs.

We conducted a comprehensive study on the existing calibration algorithms for pipeline ADC for improving the linearity. Besides all kinds of reported calibration algorithms, we do the comparison and evaluations on those. An original model-based calibration algorithm has been presented and the behavior level and the transistor level design has done. The simulations exhibits the model-based calibration algorithms are vulnerable to the accuracy matching between the pre-defined model and actual circuit characteristics, which is very difficult to control during the fabrication processes. Based on our works, we predict a more robust calibration algorithm method, which is the possible solution for improving the linearity limitation of the pipeline structure ADC to beyond 14 bit level.

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